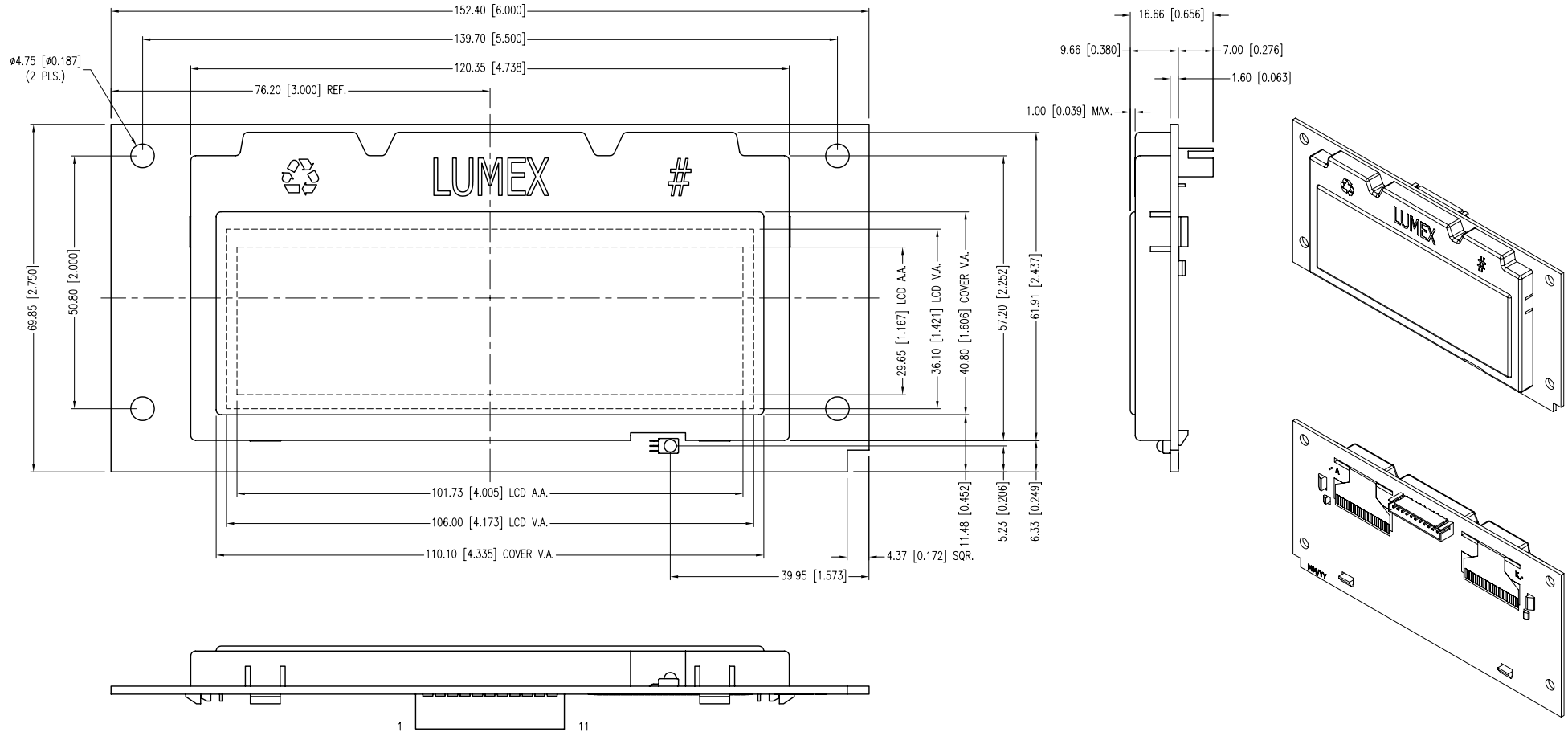


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DATE	E.C.N. NUMBER AND REVISION COMMENTS		REV.
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12.14.11	E.C.N. #10BRDR. & REDRAWN.		B



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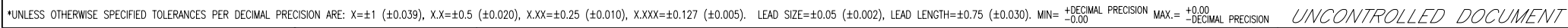
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192x56 COG GRAPHIC MODULE, DFSTN, 12:00, WHITE LED BKLT, 1/65 DUTY, 1/9 BIAS, VLCD=10V ±0.3V.

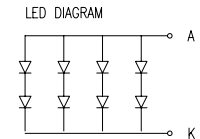
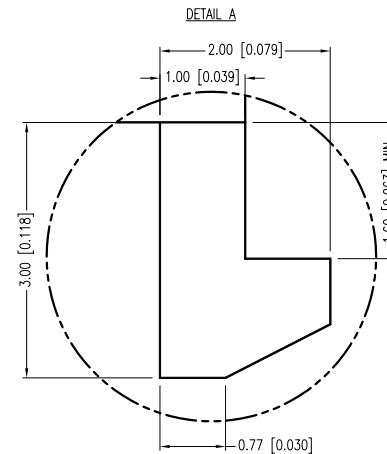
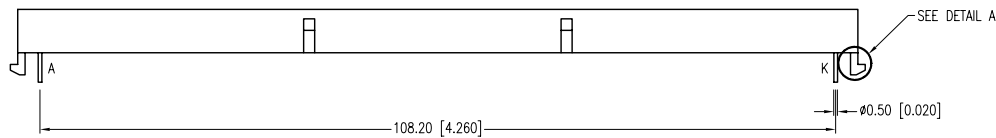
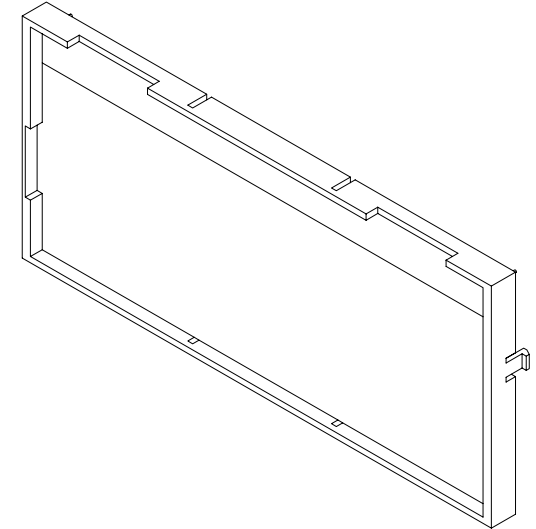
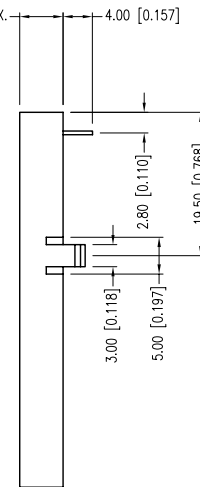
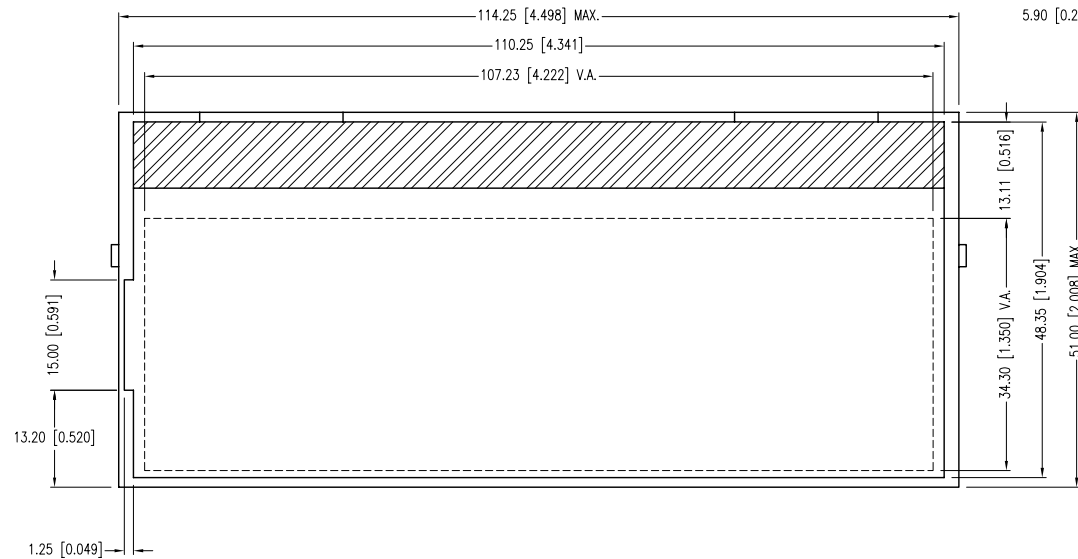
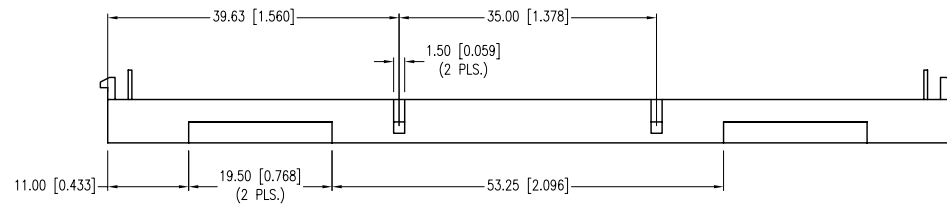
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UNIT:	mm [INCH]		Ⓟ



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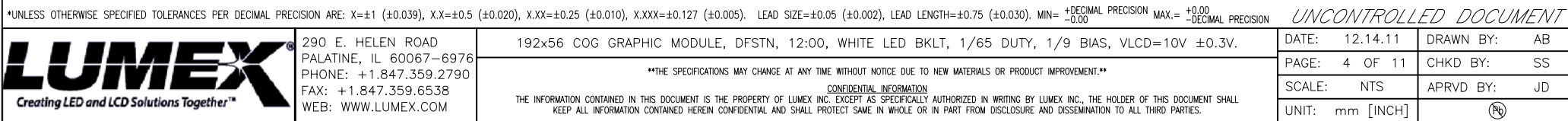
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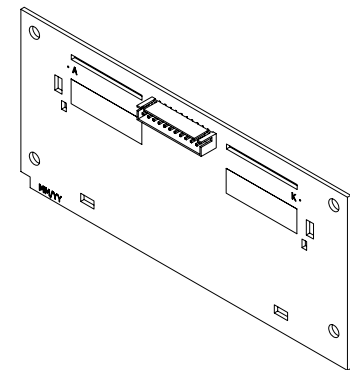
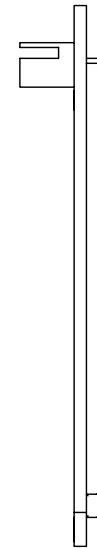
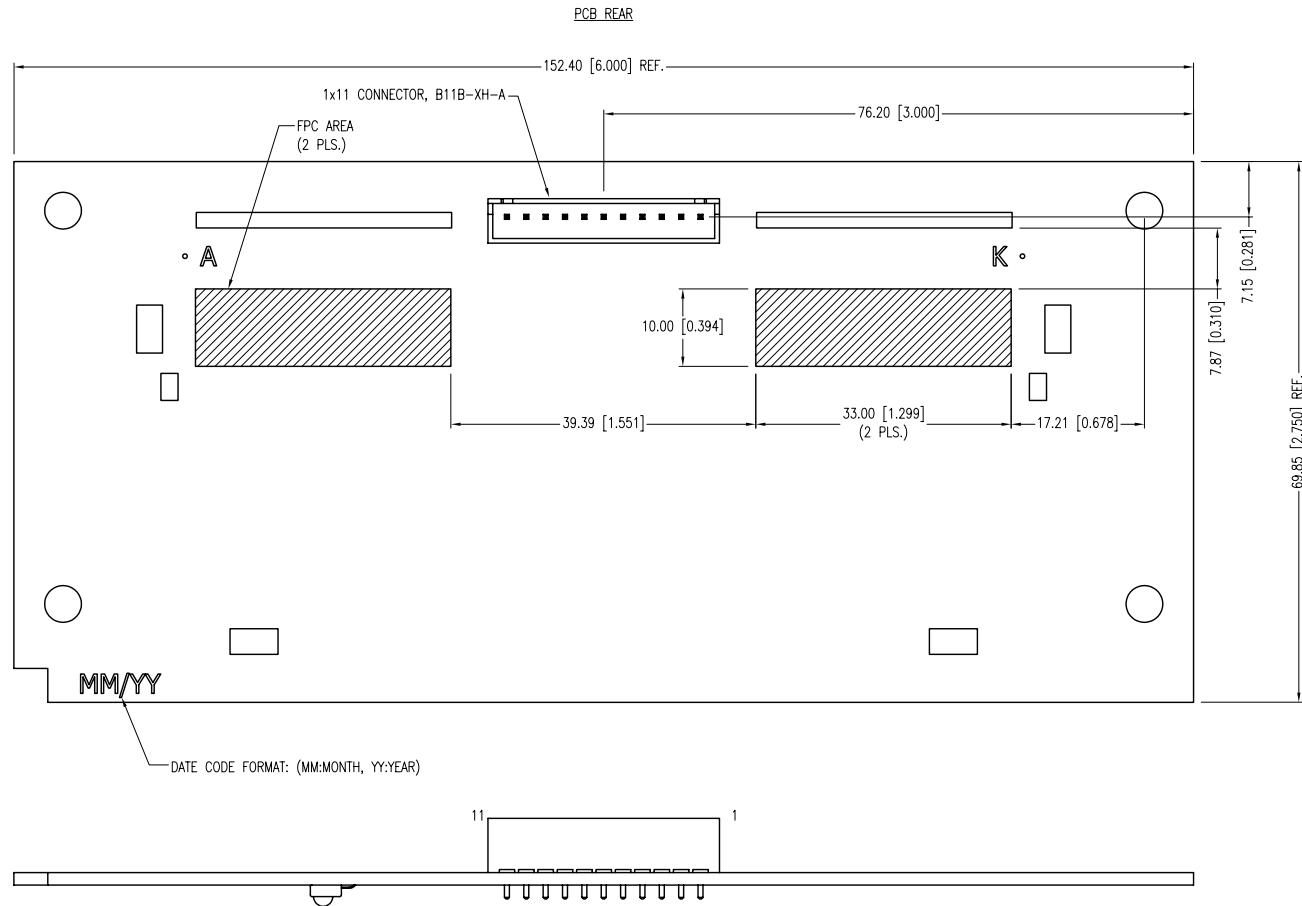
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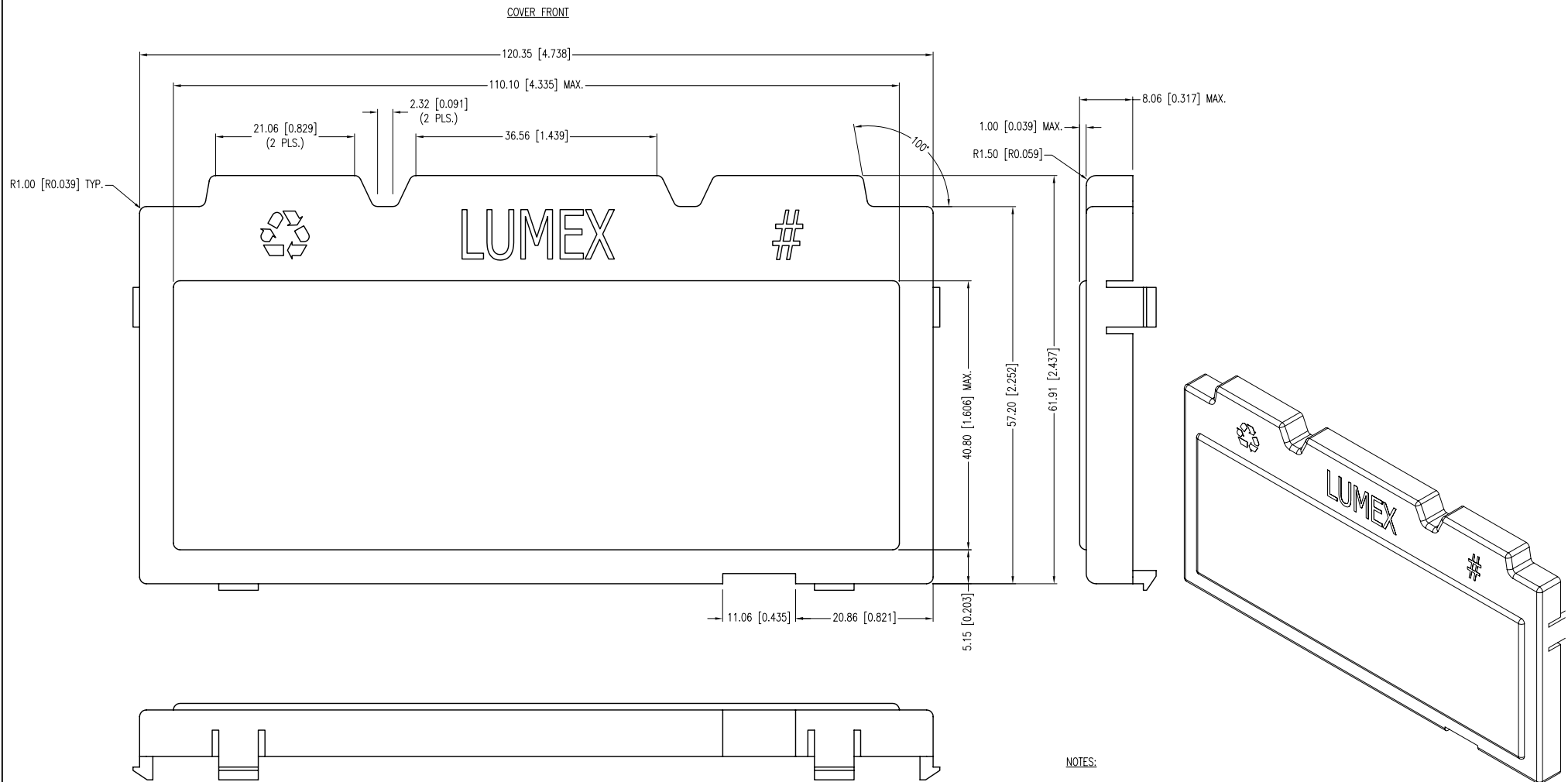
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Technical drawing of the XEMU console, showing top and side views with dimensions in inches and millimeters.

Top View Dimensions:

- Overall Width: 114.35 [4.502]
- Distance from Left Edge to First Notch: 17.62 [0.694] (2 PLS.)
- Distance between Notches: 34.00 [1.339]
- Distance from Second Notch to Right Edge: 34.00 [1.339]
- Overall Height: 51.20 [2.016]
- Distance from Top Edge to Bottom Edge of Internal Frame: 3.00 [0.118] TYP.

Side View Dimensions:

- Overall Depth: 122.35 [4.817] MIN.
- Distance from Front Edge to First Mounting Tab: 12.00 [0.472]
- Distance between Mounting Tabs: 6.00 [0.236]
- Distance from Second Mounting Tab to Rear Edge: 84.35 [3.321]

Other Features:

- Top Edge: Features a central notch and two side notches.
- Bottom Edge: Features two mounting tabs.
- Internal Frame: A dashed line indicates the internal frame structure.
- Labels: The text "XEMU" is printed in the center of the top edge.
- Orientation: A dashed line labeled "A" indicates the front/rear orientation.

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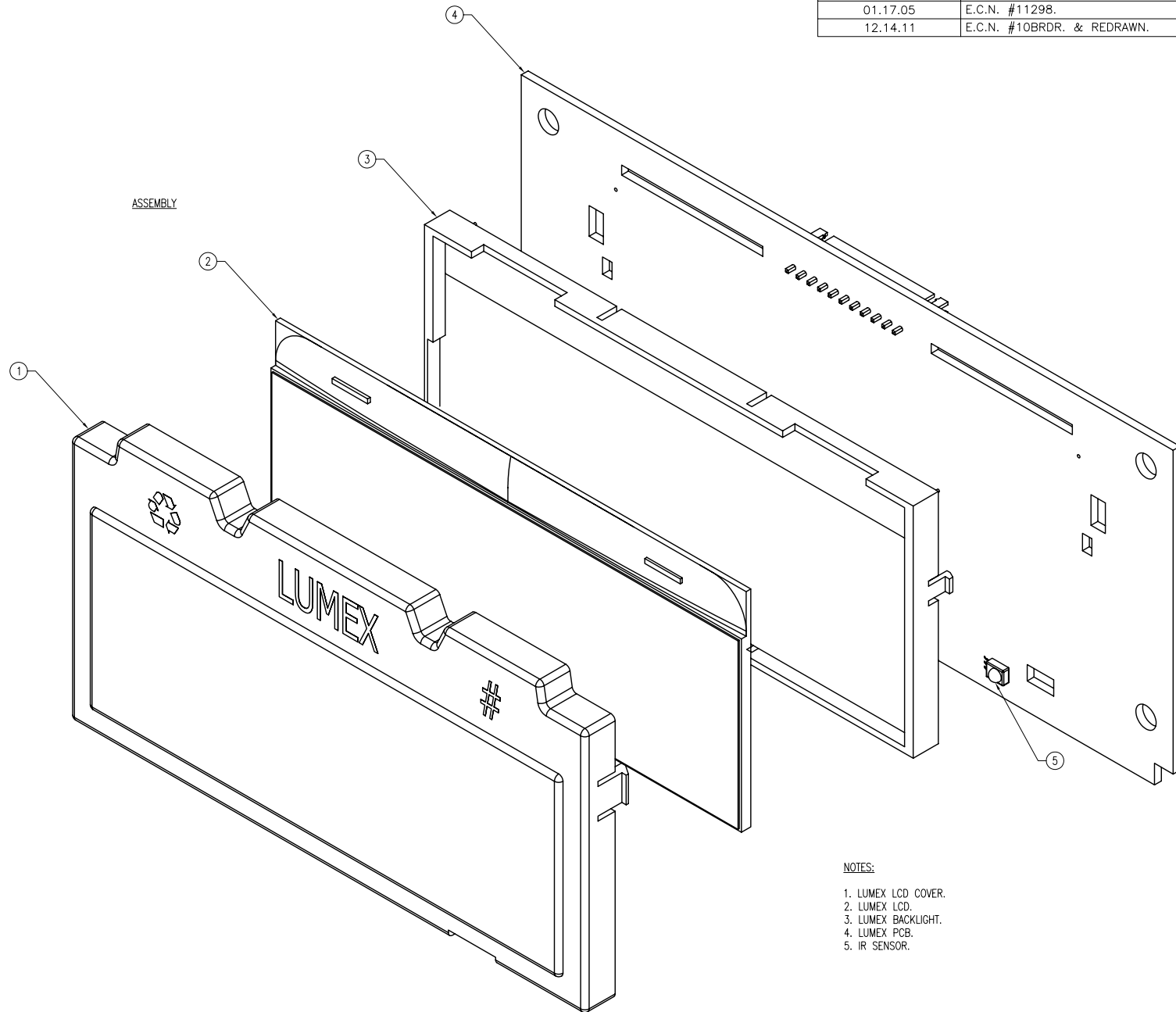
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NOTES:

1. LUMEX LCD COVER.
2. LUMEX LCD.
3. LUMEX BACKLIGHT.
4. LUMEX PCB.
5. IR SENSOR.

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PIN CONFIGURATION

PIN NO.	SYMBOL	I/O	FUNCTION
1	/CS1 MASTER	I	THIS IS THE CHIP SELECT SIGNAL. WHEN /CS1 = "L", THEN THE CHIP SELECT BECOMES ACTIVE, AND DATA/COMMAND I/O IS ENABLED.
2	/CS2 SLAVE	I	THIS IS THE CHIP SELECT SIGNAL. WHEN /CS2 = "L", THEN THE CHIP SELECT BECOMES ACTIVE AND DATA/COMMAND I/O IS ENABLED
3	/RES	I	WHEN /RES IS SET TO "L" THE SETTINGS ARE INITIALIZED THE RESET OPERATION IS PERFORMED BY THE /RES SIGNAL LEVEL
4	A0	I	THIS IS CONNECT TO THE LEAST SIGNIFICANT BIT OF THE NORMAL MPU ADDRESS BUS, AND IT DETERMINES WHETHER THE DATA OR A COMMAND A0= "H" INDICATES THAT D0-D7 ARE DISPLAY DATA. A0= "L" INDICATES THAT D0-D7 ARE CONTROL DATA.
5	D6(SCL)	I/O	D6: THE SERIAL CLOCK INPUT (SCL)
6	D7(SI)	I/O	D7: SERIAL DATA INPUT (SI);
7	VDD	PWR SUPPLY	SHARED WITH THE MPU POWER SUPPLY TERMINAL VCC
8	VSS	PWR SUPPLY	THIS IS A 0V TERMINAL CONNECTED TO THE SYSTEM GND
9	A	PWR	BACKLIGHT ANODE+
10	K	GND	BACKLIGHT CATHODE-
11	IR	I	CONNECT TO OPEN COLLECTOR PIN 2 OF IR SENSOR

LED BACKLIGHT SPECIFICATIONS

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
FORWARD VOLTAGE	Vf	5.8	6.4	7.0	V
FORWARD CURRENT	If	-	60	-	mA
POWER DISSIPATION	Pd	-	-	0.42	W
REVERSE VOLTAGE	Vr	-	-	10	V
REVERSE CURRENT	Ir	-	-	0.4	mA
LUMINOUS INTENSITY	Iv	240	300	-	cd/m ²
COLOR CHROMATICITY	X	0.26	-	0.33	-
	Y	0.26	-	0.33	-

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	STANDARD VALUE		UNIT
		MIN	MAX	
POWER SUPPLY VOLTAGE	VDD	-0.3	5.0	V
POWER SUPPLY VOLTAGE	VDD2	0.3	4.0	V
POWER SUPPLY VOLTAGE (VDD STANDARD)	V0, VOUT	0.3	18.0	V
POWER SUPPLY VOLTAGE (VDD STANDARD)	V1~V4	V0	0.3	V
INPUT VOLTAGE	VIN	-0.3	VDD+0.3	V
OPERATING TEMPERATURE	Topr	-20	+70	°C
STORAGE TEMPERATURE	Tstr	-30	+80	°C

(1) VDD≥ V1≥ V2≥ V3≥ V4.

ELECTRICAL CHARACTERISTICS

ITEM	CONDITIONS		SYMBOL	STANDARD VALUE			UNIT
				MIN	TYP	MAX	
OPERATING VOLTAGE (1)			VDD	1.8	3.0	3.3	V
OPERATING VOLTAGE (2)	RELATIVE TO VSS		VDD2	2.4	—	3.3	
INPUT VOLTAGE	HIGH		V _{INHC}	0.8*VDD	—	VDD	
	LOW		V _{ILC}	VSS	—	0.2*VDD	
OUTPUT VOLTAGE	HIGH		V _{OHc}	0.8*VDD	—	VDD	
	LOW		V _{OLc}	VSS	—	0.2*VDD	
OSCILLATOR FREQUENCY	INTERNAL	1/65, 1/33 DUTY	FOSC	17	20	24	kHz
	EXT. INPUT		FCL	17	20	24	
	INTERNAL	1/49, 1/53, 1/55, DUTY	FOSC	25	30	35	
	EXT. INPUT		FCL	25	30	35	
INTERNAL POWER	INPUT VOLTAGE	RELATIVE TO VSS	VDD2	2.4	—	3.3	V
	STEP UP OUTPUT	RELATIVE TO VSS	VOUT	—	—	16.0	
	VOLT REG.	RELATIVE TO VSS	VOUT	6.0	—	16.0	
	V. FOLLOWER	RELATIVE TO VSS	VO	4.0	10.0	13.0	
	BASE VOLT.	RELATIVE TO VSS	VR	2.07	2.10	2.13	

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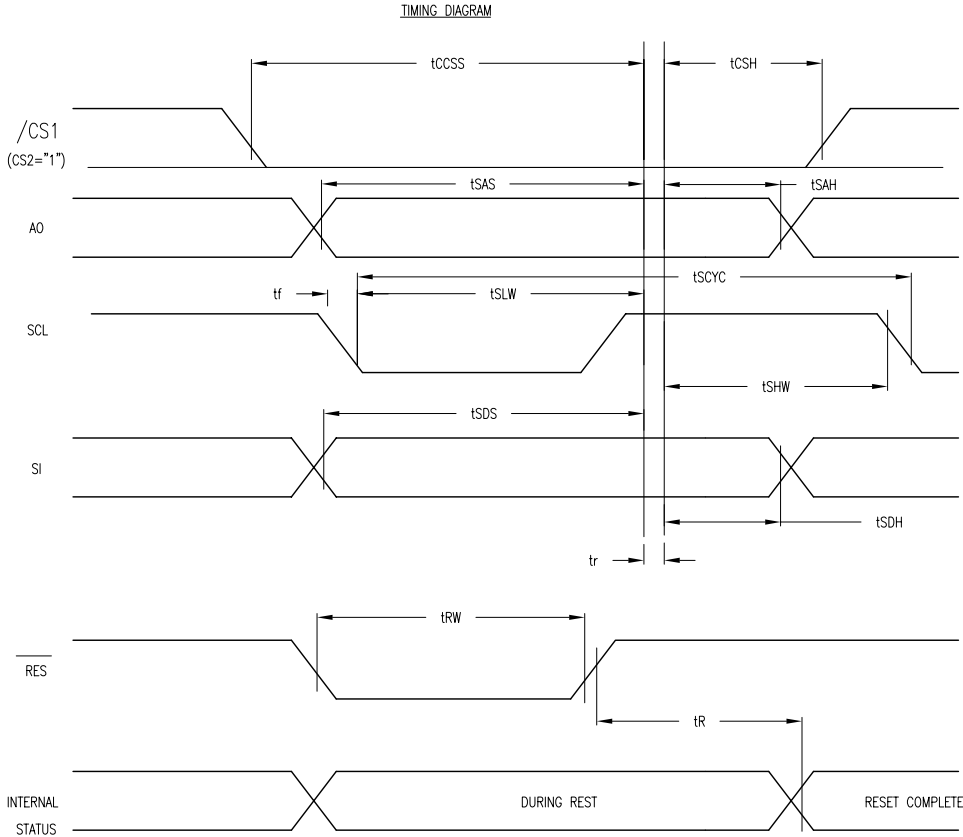
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AC CHARACTERISTICS

ITEM	SIGNAL	SYMBOL	MIN	MAX	UNIT	CONDITION
ADDRESS HOLD TIME	A0	tAH6	0	–	ns	
ADDRESS SETUP TIME		tAW6	0	–	ns	
SYSTEM CYCLE TIME	A0	tCYC6	240	–	ns	
CONTROL L PULSE WIDTH (/WR)	/WR	tEWLW	80	–	ns	
CONTROL L PULSE WIDTH (/RD)		tEWLR	80	–		
CONTROL H PULSE WIDTH (/WR)	/WR	tEWHW	80	–		
CONTROL H PULSE WIDTH (/RD)	/RD	tEWHR	140	–		
DATA SETUP TIME	D0~D7	tDS6	40	–	ns	
ADDRESS HOLD TIME		tDH6	10	–	ns	
READ ACCESS TIME		tACC6	–	70	ns	CL=100pF
OUTPUT DISABLE TIME		tOH6	5	50	ns	CL=100pF
SERIAL CLOCK PER.	SCL	Tscyc	50	–	ns	
SCL "H" PULSE WIDTH		TSHW	25	–	ns	
SCL "L" PULSE WIDTH		TSLW	25	–	ns	
ADDRESS SETUP TIME	A0	TSAS	20	–	ns	
ADDRESS HOLD TIME		tSAH	10	–	ns	
DATA SETUP TIME	SI	TSOS	20	–	ns	
DATA HOLD TIME		TSDH	10	–	ns	
CS-SCL TIME	CS	Tcss	20	–	ns	
CS-SCL TIME		Tcsh	40	–	ns	
RESET TIME		Tr	–	0.5	ns	
RESET "L" PULSE WIDTH	/RES	Trw	0.5	–	ns	

1. THE INPUT SIGNAL RISE & FALL TIME (TR, TF) ARE SPECIFIED @ 15ns OR LESS
2. ALL TIMING IS SPECIFIED USING 20% AND 80% OF VDD AS STANDARD.

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PAD NO.	CONFIGURATION
1	COM55[R55(C0-C191)]
2	COM54[R54(C0-C191)]
23	COM33[R33(C0-C191)]
24	COM32[R32(C0-C191)]
25	SEG1[C0(R0-R55)]
26	SEG2[C1(R0-R55)]
119	SEG95[C94(R0-R55)]
120	SEG96[C95(R0-R55)]
121	COM97[C96(R0-R55)]
122	COM98[C97(R0-R55)]
215	COM191[C190(R0-R55)]
216	COM192[C191(R0-R55)]
217	COM0[R0(C0-C191)]
218	COM1[R1(C0-C191)]
247	COM30[R30(C0-C191)]
248	COM31[R31(C0-C191)]

