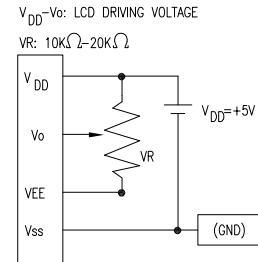


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SCALE: N/A	APRVD BY: SA
UNIT: mm [INCH]	(Pb)

PIN CONFIGURATION

PIN NO.	SYMBOL	LEVEL	FUNCTION
1~4	D0~D3	H/L	DATA BUS
5	DISP.OFF	H/L	H: ON, L: OFF
6	FLM	H	THE FLM SIGNAL INDICATES THE BEGINNING OF EACH DISPLAY CYCLE.
7	NC	-	-
8	CL1	H->L	DATA LATCH PULSE
9	CL2	H->L	DATA SHIFT CLOCK PULSE
10	V _{DD}	-	POWER SUPPLY FOR LOGIC CIRCUIT
11	V _{SS}	-	GND
12	V _{EE}	-	POWER SUPPLY FOR LCD DRIVING CIRCUIT
13	V _o	-	LCD CONTRAST VOLTAGE
14	FGND	-	FRAME



ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN.	TYP.	MAX.	
SUPPLY VOLTAGE FOR LOGIC	V _{DD} -V _{SS}	-	4.75	5.0	5.5	V
SUPPLY CURRENT FOR LOGIC	I _{DD}	NOTE 1	-	16.0	25	mA
SUPPLY VOLTAGE FOR LCD DRIVER	V _{EE} -V _{SS}	-	22.4	23.5	24.3	V
SUPPLY CURRENT FOR LCD	I _{EE}	NOTE 1	-	5.0	-	mA
INPUT VOLTAGE*	HIGH	V _{IH}	-	2.2	-	V _{DD}
	LOW	V _{IL}	-	-	0.6	V
CCFL DRIVING VOLTAGE	V _{CCFL}	Ta=25°C	-	300	-	V _{rms}
CCFL FREQUENCY	f _{CCFL}	-	-	70	85	KHz
CCFL CURRENT	I _{CCFL}	Ta=25°C	4	5	6	mA
CCFL STARTING DISCHARGE VOLTS	-	Ta=5°C	1000	-	-	V
BRIGHTNESS	-	SURFACE AREA	-	80	-	cd/m ²
CCFL OPERATING LIFETIME	-	Ta=25°C	-	10K	-	HOURS

NOTE 1: V_{DD}-V_{SS}=5.0V
V_{DD}-V_o=23.5V

*APPLIED TO TERMINALS FLM, CL1, CL2, D0~D3, DISPOFF.

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	TEST CONDITION	STANDARD VALUE		UNIT
			MIN	MAX	
SUPPLY VOLTAGE FOR LOGIC	V _{DD} -V _{SS}	Ta=25°C	-	7.0	V
SUPPLY VOLTAGE FOR LCD DRIVE	V _{DD} -V _o	Ta=25°C	-	30	V
INPUT VOLTAGE	V _I	Ta=25°C	V _{SS}	V _{DD}	V
OPERATING TEMPERATURE	T _{opr}	LCM-H	-20	70	°C
STORAGE TEMPERATURE	T _{stg}	LCM-H	-30	80	°C

*UNLESS OTHERWISE SPECIFIED TOLERANCES PER DECIMAL PRECISION ARE: X=±1 (±0.039), X.X=±0.5 (±0.020), X.XX=±0.25 (±0.010), X.XXX=±0.127 (±0.005). LEAD SIZE=±0.05 (±0.002), LEAD LENGTH=±0.75 (±0.030). MIN= ^{+DECIMAL PRECISION} -0.00 MAX= ^{+0.00} -DECIMAL PRECISION



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320 x 240 DOT MATRIX, 1/4 VGA GRAPHIC MODULE, DC-DC, 1/240 DUTY. NEGATIVE IMAGE WITH CCFL BACKLIGHT

THE SPECIFICATIONS MAY CHANGE AT ANY TIME WITHOUT NOTICE DUE TO NEW MATERIALS OR PRODUCT IMPROVEMENT.

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UNCONTROLLED DOCUMENT

Timing diagram for the 240VT device. The diagram shows the relationship between several signals over time. The top signal is CL1, followed by CL2, D3, D0, FLM, and M. The diagram includes a 52.1µs period and a T/80 time interval. Signals CL1 and CL2 are clock signals. D3 and D0 are data signals. FLM is a strobe signal. M is a master signal. The diagram shows the relationship between these signals during a data transfer cycle.

UNIT: mm [INCH]	
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