

PAGE: 1 OF 6
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NOTE: LCD MODULE WITH LED BACKLIGHT.

UNDER REVISION

SC:0.50

PART NUMBER

LCM-S12864TBWF

REV.

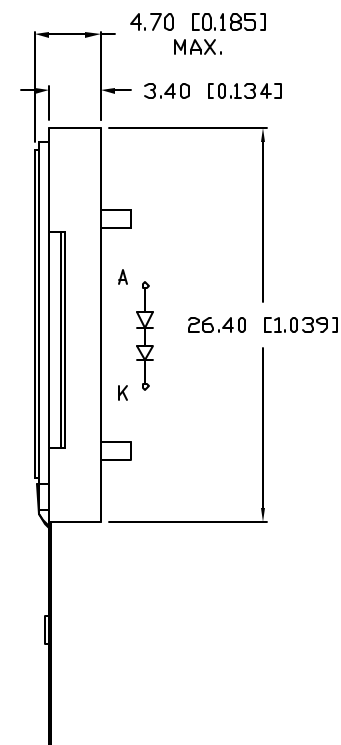
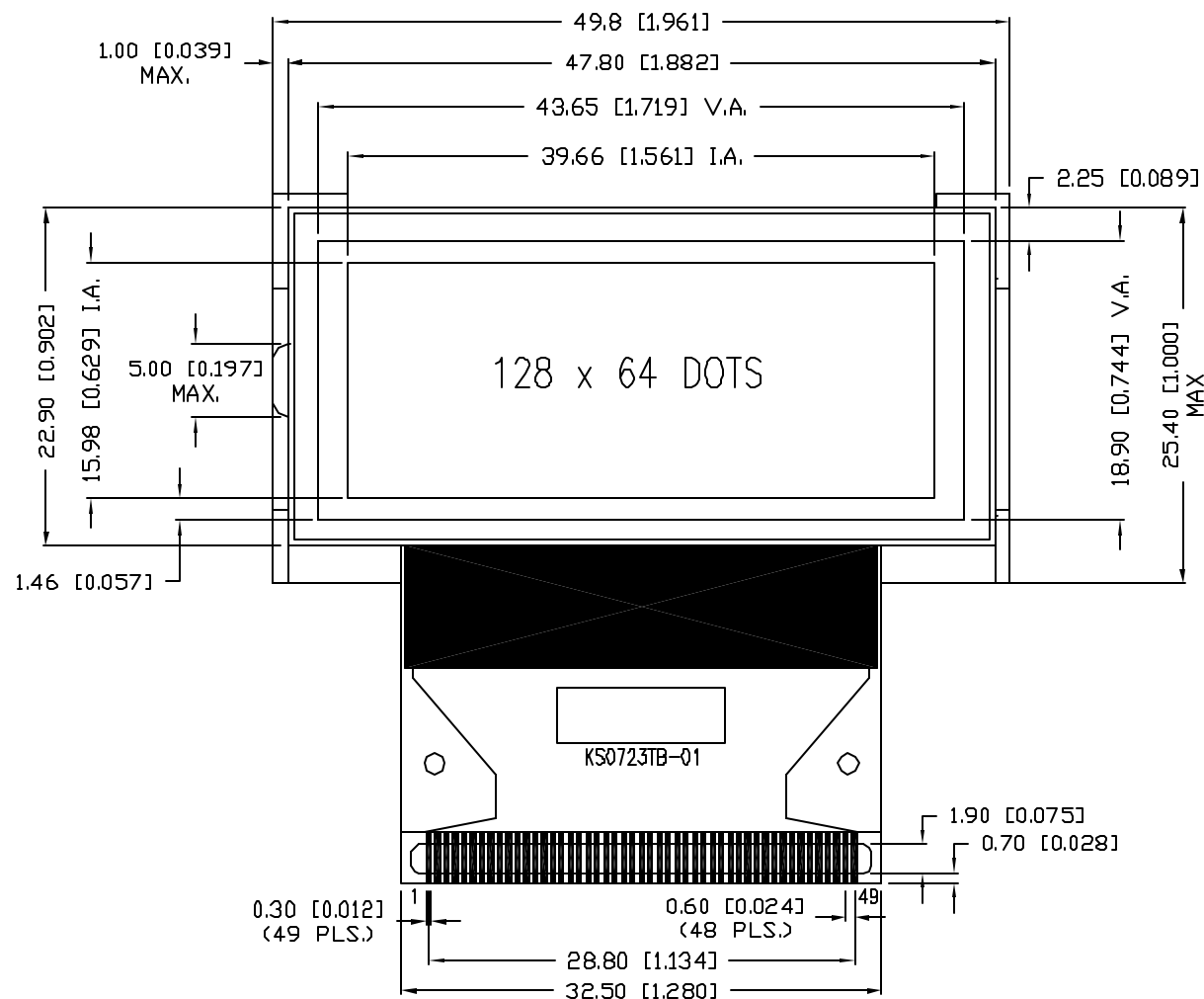
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REV.	E.C.N. NUMBER AND REVISION COMMENTS
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-0.01
MAX.=+0.00
-0.01

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LCM-S12864TBWF

128 x 64 TAB TYPE GRAPHIC LCD MODULE, FSTN, 6:00 VIEW,
TRANSFLECTIVE, 1/65 DUTY, 1/9 BIAS, VLCD=10V TYP.,
INTERFACE: SERIAL OR PARALLEL. GREEN 565nm BACKLIGHT.

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RELIABILITY NOTE

OUR MANY YEARS OF EXPERIENCE DATA ACCUMULATION INDICATE THAT
SOLDER HEAT IS A MAJOR CAUSE OF EARLY AND FUTURE FAILURE.
PLEASE PAY ATTENTION TO YOUR SOLDERING PROCESS.



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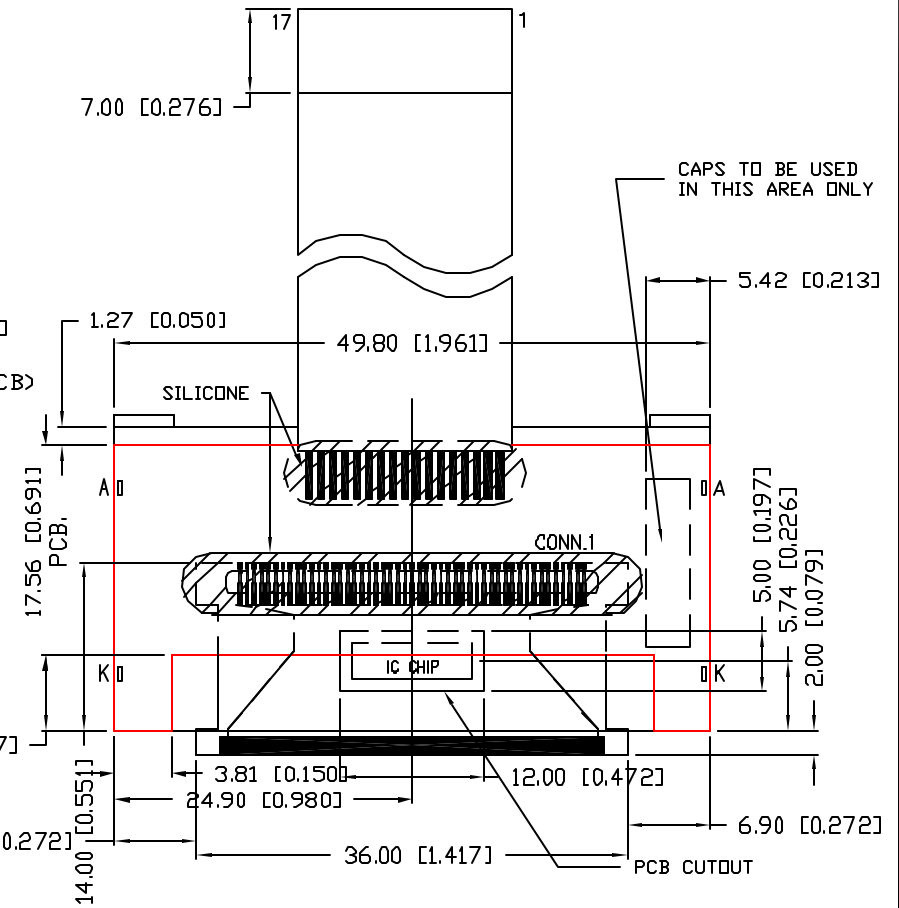
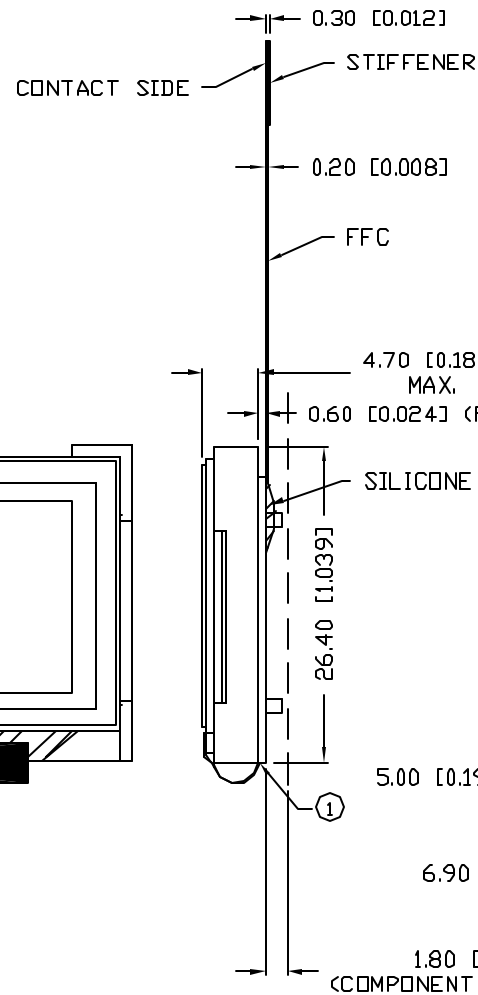
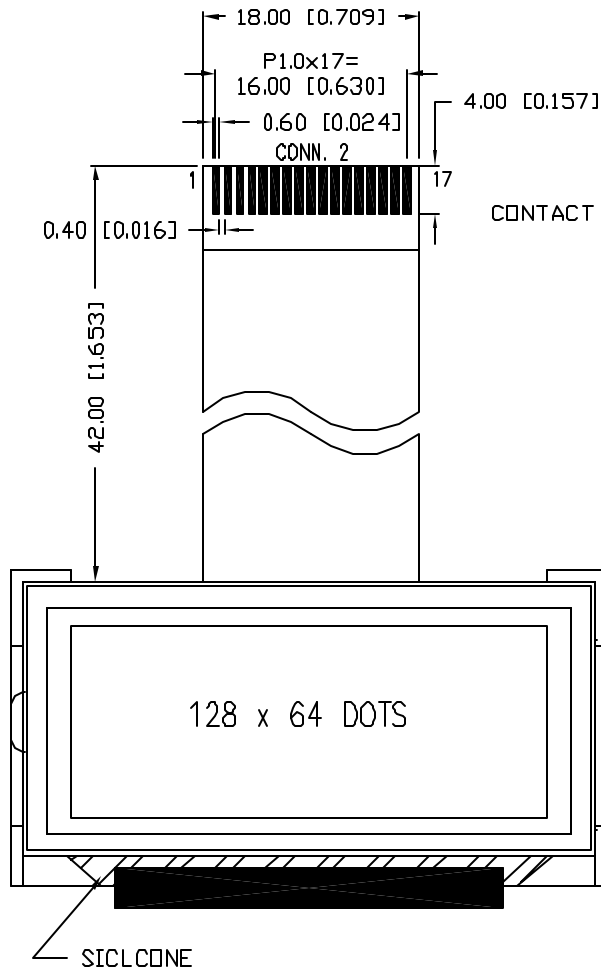
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NOTES:

1. TAB BETWEEN BACKLIGHT AND PCB.

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128 x 64 TAB TYPE GRAPHIC LCD MODULE, FSTN, 6:00 VIEW, TRANSFLECTIVE, 1/65 DUTY, 1/9 BIAS, VLCD=10V TYP., INTERFACE: SERIAL OR PARALLEL, GREEN 565nm BACKLIGHT.

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PIN CONFIGURATION			THE LCD DRIVER DUTY RATIO DEPENDS ON THE FOLLOWING TABLE.		
	DUTY1, DUTY0	H/L	DUTY1	DUTY0	DUTY RATIO
26, 27			L	L	1/33
			L	H	1/49
			H	L	1/55
			H	H	1/65
28~35	DB7~DB0	H/L	8-BIT BI-DIRECTIONAL DATA BUS, STANDARD 8-BIT MICROPROCESSOR BUS. WHEN SERIAL INTERFACE SELECTED (PS=L); DB0 TO DB5: HIGH IMPEDANCE; DB6: SERIAL INPUT CLOCK (SCLK); DB7: SERIAL INPUT DATA (SID); WHEN CHIP SELECT IS NOT ACTIVE, DB0~DB7 MAY BE HIGH IMPEDANCE.		
36	E-RDB	H/L	READ/WRITE EXECUTION CONTROL PIN.		
			C68	MPU TYPE	E-RDB DESCRIPTION
			H	6800-SERIES	E
			L	8080-SERIES	/RDB
37	RW-WRB	H/L	READ/WRITE EXECUTION CONTROL PIN.		
			C68	MPU TYPE	E-RDB DESCRIPTION
			H	6800-SERIES	RW
			L	8080-SERIES	WRB
38	RS	H/L	REGISTER SELECT INPUT PIN. H: DB0~DB7 ARE DISPLAY DATA, L: DB0~DB7 ARE CONTROL DATA.		
39	RESETB	H/L	RESET INPUT, WHEN RESETB IS "L", INITIALIZATION IS EXECUTED.		
40, 41	CS2, CS1B	H/L	CHIP SELECT. DATA I/O IS ENABLED ONLY WHEN CS1B IS "L" AND CS2 IS "H" WHEN CHIP SELECT IS NON-ACTIVE, DB0~DB7 MAY BE HIGH IMPEDANCE.		
42	TEST4	H/L	FOR IC CHIP TESTING. SET PIN TO OPEN.		
43	DISP	H/L	LCD DISPLAY BLANKING CONTROL INPUT/OUTPUT. WHEN IC CHIP IS USED IN MASTER/SLAVE MODE, THE "DISP" PIN MUST BE CONNECTED TO EACH OTHER. H: OUTPUT, L: INPUT.		
44	CL	H/L	DISPLAY CLOCK INPUT/OUTPUT PIN. WHEN THE IC CHIP IS USED IN MASTER/SLAVE MODE THE CL PINS MUST BE CONNECTED TO EACH OTHER.		
45	M	H/L	LCD AC SIGNAL INPUT/OUTPUT PIN. WHEN THE IC CHIP IS USED IN MASTER/SLAVE MODE, THE M PINS MUST BE CONNECTED TO EACH OTHER. H: OUTPUT, L: INPUT.		
46~48	TEST3~TEST1	H/L	PINS USED FOR IC TESTING. SET TO OPEN.		
49	DUMMY	-	NOT USED		

CONN. 1			FUNCTION						
PIN NO.	SYMBOL	LEVEL	NOT USED						
1	DUMMY	-							
2	INTRS	H/L	INTERNAL RESISTORS SELECT, SELECTS RESISTORS FOR ADJUSTING VO VOLTAGE LEVEL, ONLY VALID IN MASTER OPERATION. H: INTERNAL RESISTORS, L: EXTERNAL RESISTORS. VO VOLTAGE IS CONTROLLED BY VR PIN AND EXTERNAL RESISTIVE DIMMER.						
3	HPMB	H/L	POWER CONTROL FOR LCD DRIVER H: NORMAL MODE, L: HIGH POWER MODE. VALID IN MASTER OPERATION.						
4	PS	H/L	PARALLEL/SERIAL DATA INPUT SELECT INPUT.						
			PS	CHIP SELECT	INTERFACE MODE	DATA INSTRUCTION	DATA	R/W	SERIAL CLOCK
			H	CS1B, CS2	PARALLEL	RS	DB0~DB7	E-RDB RW-WRB	-----
			L	CS1B, CS2	SERIAL	RS	SID (DB7)	WRITE ONLY	SCLK (DB6)
5	C68	H/L	MICROPROCESSOR INTERFACE SELECT INPUT IN PARALLEL MODE. H: 6800-SERIES MPU INTERFACE, L: 8080-SERIES MPU INTERFACE.						
6	CLS	H/L	BUILT-IN OSCILLATOR CIRCUIT ENABLE/DISABLE SELECT. H: ENABLE, L: DISABLE (EXTERNAL DISPLAY CLOCK INPUT TO CL PIN.)						
7	MS	H/L	MASTER/SLAVE OPERATION SELECT. H: MASTER MODE, L: SLAVE MODE.						
8	VR	H/L	VO VOLTAGE ADJUST PIN. ONLY VALID WHEN INTRS = L.						
9,10~13	VO,V4~V1	-	LCD DRIVER SUPPLY VOLTAGES						
14	REF	H/L	SELECT EXTERNAL VREF VOLTAGE VIA VEXT PIN. L: USING EXTERNAL VREF, H: USING INTERNAL VREF.						
15	VEXT	-	EXTERNAL-INPUT REFERENCE VOLTAGE FOR INTERNAL VOLTAGE REGULATOR. ONLY VALID WHEN EXTERNAL VREF IS USED (REF=L) WHEN USING INTERNAL VREF, THIS PIN IS OPEN.						
16	C2-	-	CAPACITOR 2 NEGATIVE CONNECTION FOR VOLTAGE CONVERTOR						
17	C2+	-	CAPACITOR 2 POSITIVE CONNECTION FOR VOLTAGE CONVERTOR						
18	C1+	-	CAPACITOR 1 POSITIVE CONNECTION FOR VOLTAGE CONVERTOR						
19	C1-	-	CAPACITOR 1 NEGATIVE CONNECTION FOR VOLTAGE CONVERTOR						
20	C3+	-	CAPACITOR 3 POSITIVE CONNECTION FOR VOLTAGE CONVERTOR						
21	C4+	-	CAPACITOR 4 POSITIVE CONNECTION FOR VOLTAGE CONVERTOR						
22	VOU	-	VOLTAGE CONVERTER INPUT/OUTPUT PIN. CONNECT TO VSS THRU CAPACITOR.						
23	VSS	-	GROUND						
24	VCI	H/L	REFERENCE VOLTAGE FOR VOLTAGE CONVERTER CIRCUIT FOR LCD DRIVING. WHETHER INTERNAL VOLTAGE CONVERTER USED OR NOT, THIS PIN IS FIXED. RECOMMENDED VOLTAGE RANGE: 2.4V<VCI<5.5V.						
25	VDD	-	POWER SUPPLY						

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CONN. 2

PIN NO.	SYMBOL	FUNCTION						
1	CS1B	CHIP SELECT INPUT PIN. DATA / INSTRUCTION I/O IS ENABLED ONLY WHEN CS1B IS "L" AND CS2 IS "H". WHEN CHIP SELECT IS NON-ACTIVE, DB0 TO DB7 MAY BE HIGH IMPEDANCE.						
2	RESETB	RESET INPUT PIN. WHEN RESETB IS "L", INITIALIZATION IS EXECUTED.						
3	RS	REGISTER SELECT INPUT PIN. -RS= "H" :DB0 TO DB7 ARE DISPLAY DATA -RS= "L" :DB0 TO DB7 ARE CONTROL DATA.						
4	RW-WRB	READ/WRITE EXECUTION CONTROL PIN						
		<table><tr><th>C68</th><th>MPU TYPE</th><th>RW-WRB</th><th>DESCRIPTION</th></tr><tr><td>H</td><td>6800 SERIES</td><td>RW</td><td>READ/WRITE CONTROL INPUT PIN -RW= "H" :READ -RW= "H" :WRITE</td></tr></table>	C68	MPU TYPE	RW-WRB	DESCRIPTION	H	6800 SERIES
C68	MPU TYPE	RW-WRB	DESCRIPTION					
H	6800 SERIES	RW	READ/WRITE CONTROL INPUT PIN -RW= "H" :READ -RW= "H" :WRITE					
5	E-RDB	READ/WRITE EXECUTION CONTROL PIN						
		<table><tr><th>C68</th><th>MPU TYPE</th><th>RW-WRB</th><th>DESCRIPTION</th></tr><tr><td>H</td><td>6800 SERIES</td><td>E</td><td>READ/WRITE CONTROL INPUT PIN -RW= "H" :WHEN E IS "H", DB0 TO DB7 ARE IN AN OUTPUT. -RW= "L" :THE DATA ON DB0 TO DB7 ARE LATCHED AT THE FALLING EDGE OF THE E.</td></tr></table>	C68	MPU TYPE	RW-WRB	DESCRIPTION	H	6800 SERIES
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H	6800 SERIES	E	READ/WRITE CONTROL INPUT PIN -RW= "H" :WHEN E IS "H", DB0 TO DB7 ARE IN AN OUTPUT. -RW= "L" :THE DATA ON DB0 TO DB7 ARE LATCHED AT THE FALLING EDGE OF THE E.					
6~13	DB7~DB0	8-BIT BI-DIRECTIONAL DATA BUS THAT IS CONNECTED TO THE STANDARD 8-BIT MICROPROCESSOR DATA BUS. WHEN THE SERIAL INTERFACE SELECT (PS="L") DB0 TO DB5: HIGH IMPEDANCE; DB6: SERIAL INPUT CLOCK (SCLK); DB7: SERIAL INPUT DATA (SID); WHEN CHIP SELECT IS NOT ACTIVE, DB0 TO DB7 MAY BE HIGH IMPEDANCE.						
14	VDD	POWER SUPPLY						
15	VSS	GROUND						
16	LED+	POWER SUPPLY FOR THE BACKLIGHT: POSITIVE TERMINAL.						
17	LED-	POWER SUPPLY FOR THE BACKLIGHT: NEGATIVE TERMINAL.						

NOTE: FOR DETAIL TIMING CHARTS, TIMING DIAGRAMS, SERIAL/PARALLEL INTERFACE OPTIONS AND LCD CONNECTION METHODS, PLEASE REFER TO THE IC SPECS.

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ELECTRICAL CHARACTERISTICS			VSS=0V, VDD=2.4V~5.5V, Ta=0~50°C			
ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN.	TYP.	MAX.	
OPERATING VOLTAGE (1)	V _{DD}	—	2.4	—	5.5	V
OPERATING VOLTAGE (2)	V _O	—	4.5	—	15.0	V
INPUT VOLTAGE	HIGH	V _{IH}	—	0.8*V _{DD}	—	V _{DD}
	LOW	V _{IL}	—	V _{SS}	—	0.2*V _{DD}
OUTPUT VOLTAGE	HIGH	V _{OH}	I _{OH} =-0.5mA	0.8*V _{DD}	—	V _{DD}
	LOW	V _{OL}	I _{OL} =0.5mA	V _{SS}	—	0.2*V _{DD}
INPUT LEAKAGE CURRENT	I _{IL}	V _{IN} =V _{DD} OR V _{SS}	-1.0	—	+1.0	μA
OUTPUT LEAKAGE CURRENT	I _{OZ}	V _{IN} =V _{DD} OR V _{SS}	-3.0	—	+3.0	μA
LCD DRIVER ON RESISTANCE	R _{ON}	Ta=25°C, V _O =0V	—	2.0	3.0	kΩ
OSCILLATOR FREQUENCY	INTERNAL	F _{OSC}	Ta=25°C,	32.7	43.6	kHz
	EXTERNAL	F _{CL}	DUTY=1/85	4.09	5.45	
VOLTAGE CONVERTER INPUT VOLTAGE	V _{CI}	x2	2.4	—	5.5	V
			x3	—	5.3	
			x4	—	4.0	
			x5	—	3.2	
VOLTAGE CONVERTER OUTPUT VOLTAGE	V _{OUT}	x2/x3/x4/x5 VOLTAGE CONVERSION	95	99	—	%
VOLTAGE REGULATOR OPERATING VOLTAGE	V _{OUT}	—	6.0	—	16	V
VOLTAGE FOLLOWER OPERATING VOLTAGE	V _O	—	4.5	—	15	V
REFERENCE VOLTAGE	V _{REF}	Ta=25°C, -0.05%/°C	2.04	2.1	2.16	V
LED BACKLIGHT	VOLTAGE	V _f	I _f =20mA/NODE	—	4.1	4.5
	CURRENT	I _f	—	—	20	mA
	POWER CONSUMPTION	P _D	—	—	82	mW
	LUMINOUS	L	I _f =20mA/NODE	—	18	—

ABSOLUTE MAXIMUM RATINGS					
ITEM	SYMBOL	TEST CONDITION	STANDARD VALUE		UNIT
SUPPLY VOLTAGE RANGE	V _{DD}	Ta=25°C	-0.3	7.0	V
	V _{LCD}	—	+0.3	17.0	V
INPUT VOLTAGE	V _{IN}	Ta=25°C	-0.3	V _{DD} +0.3	V
OPERATING TEMPERATURE	T _{opr}	—	0	50	°C
STORAGE TEMPERATURE	T _{stg}	—	-10	60	°C

WARNING:
IF SUPPLY VOLTAGE EXCEEDS ITS ABSOLUTE MAXIMUM RANGE, THIS MODULE MAY BE DAMAGED PERMANENTLY!

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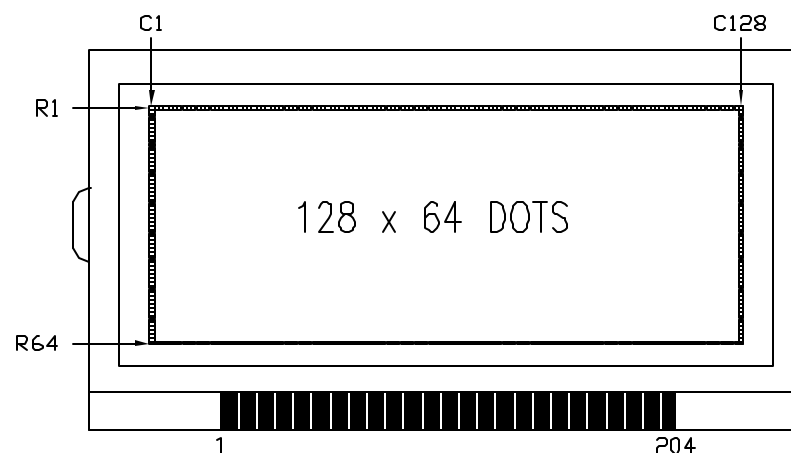
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PAD CONFIGURATION GRAPHIC DIMENSION

PAD #	PAD CONFIGURATION
1	NC
2	NC
3	COM33[R33(C1-C128)]
4	COM34[R34(C1-C128)]
33	COM63[R63(C1-C128)]
34	COM64[R64(C1-C128)]
35	NC
36	SEG1[C1(R1-R64)]
37	SEG2[C2(R1-R64)]
162	SEG127[C127(R1-R64)]
163	SEG128[C128(R1-R64)]
164	NC
167	NC
168	COM32[R32(C1-C128)]
169	COM31[R31(C1-C128)]
198	COM2[R2(C1-C128)]
199	COM1[R1(C1-C128)]
200	NC
204	NC

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