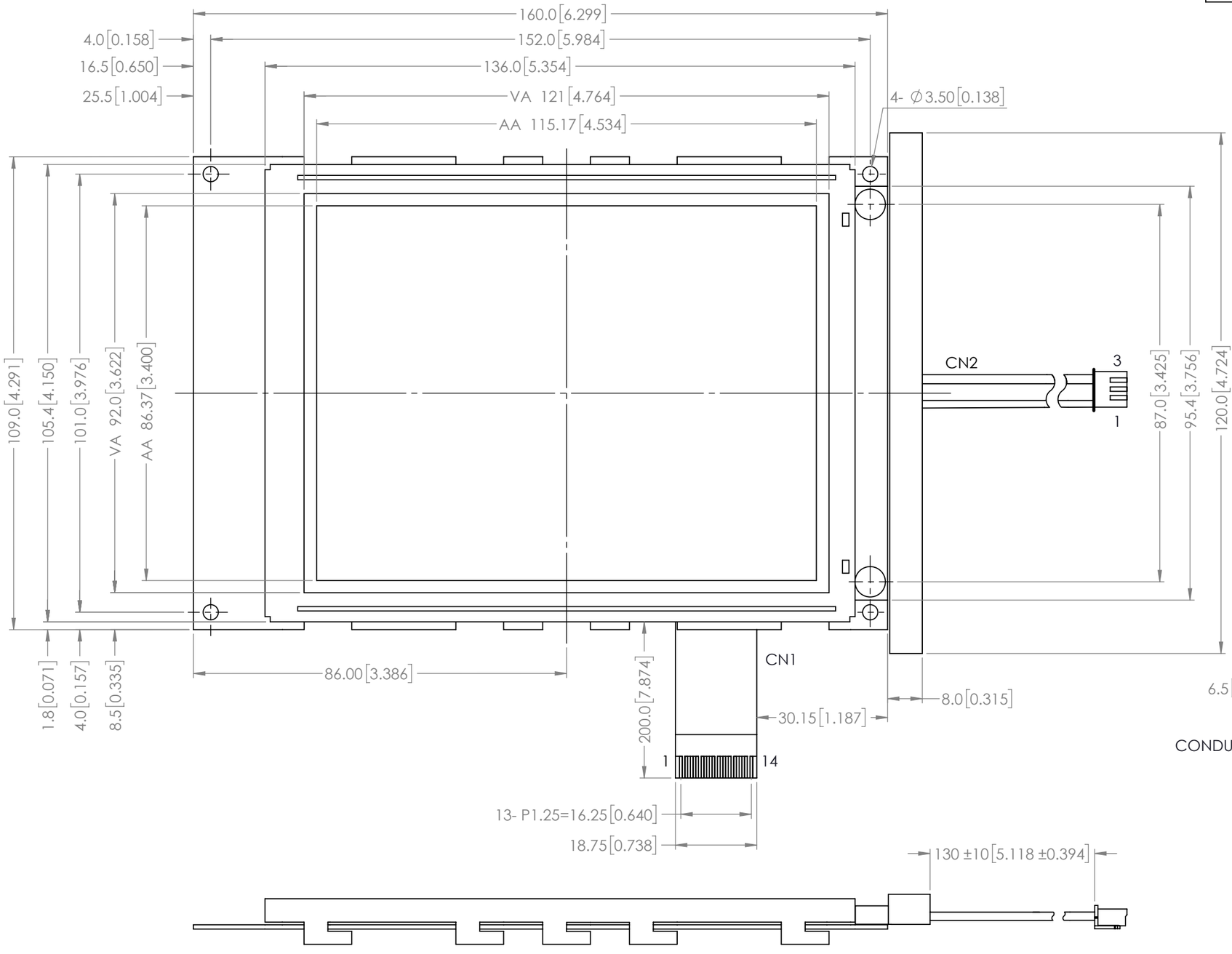
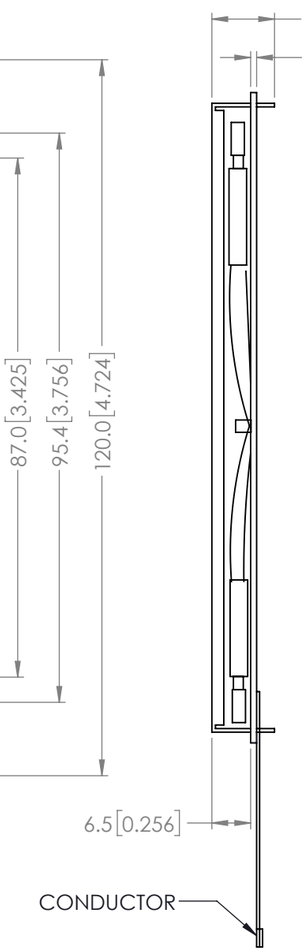
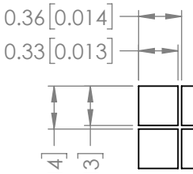
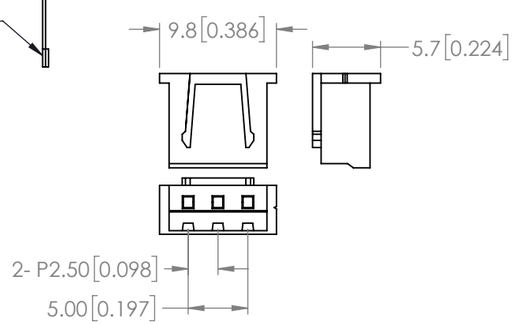
PART NUMBER	LCM-S320240GSN/B-L	REV	--









CN1

PIN NO	SIGNAL
1	DB0
2	DB1
3	DB2
4	DB3
5	DISPOFF
6	FLM
7	NC
8	LP
9	CP
10	VDD
11	VSS
12	VEE
13	V0
14	FGND

CN2

1	BL1
2	NC
3	BL2

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120(L)*168(W)*11(H)mm, 320x240 DOT MATRIX, 1/4 VGA GRAPHIC MODULE, DC-DC, 1/240 DUTY, STN NEGATIVE IMAGE WITH LED BACKLIGHT.

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PAGE : 1 OF 4	CHKD BY : R.C.
SCALE : NTF	APRVD BY : E.C.
UNIT : mm [INCH]	Pb

MECHANICAL SPECIFICATION

Module Size	160.0(W)mm×109.0(H)mm×11.0(D)mm Max
Dot Size	0.33(W)mm×0.33(H)mm
Dot Pitch	0.36(W)mm×0.36(H)mm
Resolution	320(W)×240(H) Dots Matrix
Duty Ratio	1/240 Duty

ABSOLUTE MAXIMUM RATING

(1) ELECTRICAL ABSOLUTE RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT
POWER SUPPLY FOR LOBIC	V_{DD}-V_{SS}	-0.3	7.0	VOLT
POWER SUPPLY FOR LCD	V_{DD}-V_O	0	30.0	VOLT
INPUT VOLTAGE	V1	-0.3	V_{DD}	VOLT
LED POWER DISIPATION	P_{AD}	--	720	mW
LED FORWARD CURRENT	I_{AF}	--	200	mW
LED REVERSE VOLTAGE	V_R		5	V

(2) ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	NORMAL TEMPERATURE				WIDE TEMPERATURE			
	OPERATING		STORAGE		OPERATING		STORAGE	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
AMBIENT TEMPERATURE	0 °C	+50 °C	-20 °C	+70 °C	-20 °C	+70 °C	-30 °C	+80 °C
HUMIDITY(WITHOUT CONDENSATION)	NOTE 2 , 4		NOTE 3 , 5		NOTE 4 , 5		NOTE 4 , 6	

Note 2 Ta≦50℃: 80% RH max
Ta>50℃: Absolute humidity must be lower than the humidity of 85%RH at 50℃
Note 3 Ta at -20℃ will be<48hrs at 70℃will be<120hrs when humidity is higher than 75%.
Note 4 Background color changes slightly depending on ambient temperature. This phenomenon is reversible.
Note 5 Ta≦70℃: 75RH max
Ta>70℃: absolute humidity must be lower than the humidity of 75%RH at 70℃
Note 6 Ta at -30℃ will be <48hrs, at 80 ℃ will be <120hrs when humidity is higher than 75%.

INTERFACE PIN ASSIGNMENT

PIN NO.	PIN OUT	Description
1	D0	Data input signal
2	D1	Data input signal
3	D2	Data input signal
4	D3	Data input signal
5	DispOFF	Display OFF. Active LOW.
6	FRM	Frame start signal (Data signal fromthe common driver shift register)
7	NC	No Connection.
8	CL1	Common driver data shift signal: alsolatches the data ofthe line immediately above.
9	CL2	Clock pulse for segment shift register
10	VDD	Logic supply voltage
11	VSS	GND
12	VEE	Negative power supply voltage
13	Vo	Power supply for LCD panel
14	FGND	Frame ground

PIN NO.	PIN OUT	Description
1	BL1/A	LED Power (+)
2	NC	No Connection.
3	BL2/K	LED Power (-)

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ELECTRICAL CHARACTERISTICS

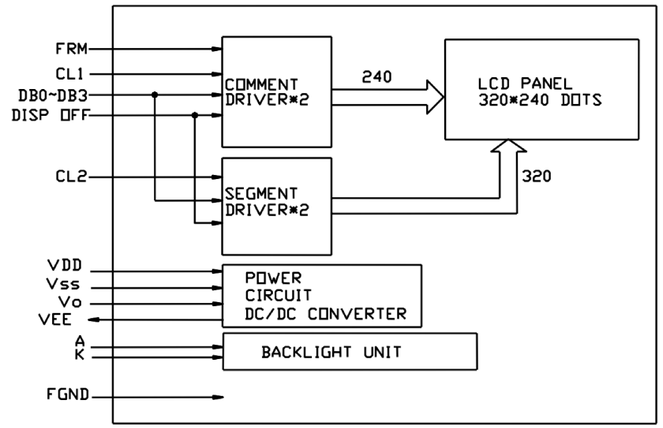
Item	Symbol	Condition	Min.	Typ	Max.	Unit	note
Power Supply for Logic	V_{DD}-V_{SS}	-	4.5	5.0	5.5	Volt	
Power Supply for LCD Drive	V_{EE}-V_{SS}	-	-21.6	-22.1	-22.7	Volt	
Input Voltage	V_{IL}	L level	0	-	0.6	Volt	
	V_{IH}	H level	2.2	-	V_{DD}	Volt	
	V_{DD}-V_O	Ta＝0℃	-	22.7	-	Volt	
		Ta＝25℃	-	24.3	-		
		Ta＝50℃	-	25.8	-		
Power Supply Current for LCM	I_{DD}	V_{DD} =5.0V V_{DD}-V_O =24.3V	34.9	31.3	-	mA	
	I_{EE}		-	3.6	-		
LED Forward Voltage	V_F	If＝160 mA	-	3.2	3.4	Volt	
LED Forward Current	I_F	-	-	160	-	mA	
LED Reverse Current	I_R	VR=5V	-	-	0.3	mA	

OPTICAL CHARACTERISTICS

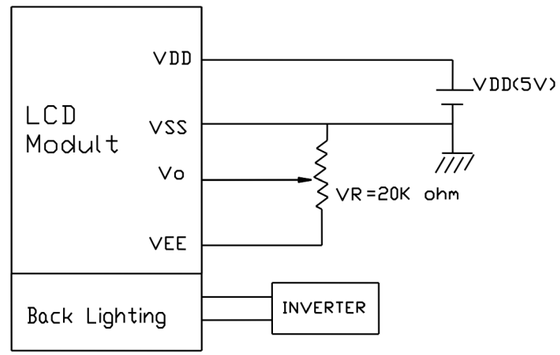
Item	Symbol	Condition	Min.	Typ	Max.	Unit	note
Viewing angle range	Φf(12 o'clock)	When Cr≧ 1.4	-	20	-	Degree	9,10
	Φb(6 o'clock)		-	40	-		
	Φl(9 o'clock)		-	30	-		
	Φr(3 o'clock)		-	30	-		
Rise Time	Tr	V_{DD}-V_O =24.3V Ta=25℃		175		ms	
Fall Time	Tf			170			
Frame frequency	Frm		-	64	-	Hz	8,10
Contrast	Cr		-	4.5	-		7
The Brightness Of Backlight	L	IF=160 mA	160	200	-	cd/㎡	
Peak Emission Wavelength	λP		X=0.29 Y=0.30	X=0.31 Y=0.32	X=0.33 Y=0.34	nm	

BLOCK DIAGRAM

(1) Built-inM-clock generatingcircuit, Userdo not haveto supplier M-clock.



(2) POWER SUPPLY



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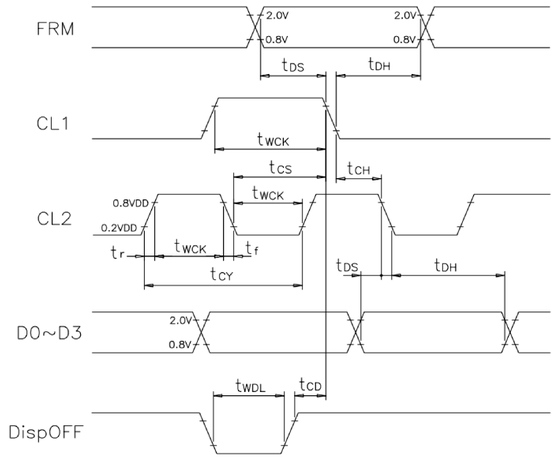
UNIT： mm [INCH]	Pb

TIMING CHARACTERISTICS

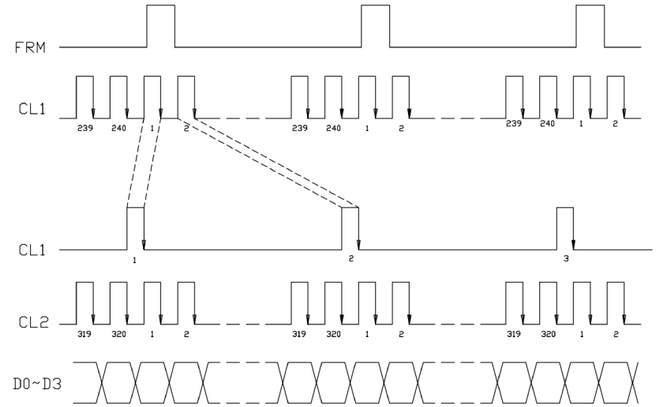
(1) Segment interface timing: (VSS=0V, VDD=2.7V to 5.0V, Ta=-20 to 70℃)

Item	Symbol	Test Condition	Min.	Max.	Unit
Clock cycle time	t_{CY}	Duty = 50%	250	-	ns
Clock Pulse Width	t_{WCK}		95	-	ns
Data Set Up Time	t_{DS}		65	-	ns
Data Hold Time	t_{DH}		65	-	ns
Latch pulse 'H' width	t_{WCK}		95	-	ns
Input signal Rise/Fall Time	t_r, t_f		-	30	ns
Clock Set Up Time	t_{CS}		120	-	ns
Clock hold time	t_{CH}		120	-	ns
FRM set-up time	t_{DS}		30		ns
FRM hold time	t_{DH}		30		ns
DispOFF clear time	t_{CD}		100	-	ns
DispOFF 'L' pulse width	t_{WDL}		1.2	-	μs



DISPLAY PATTERN

(1) Relationship between every signal



	SEG1	SEG2	SEG3	SEG4	.....	SEG317	SEG318	SEG319	SEG320
COM1	D3	D2	D1	D0	.....	D3	D2	D1	D0
COM2	D3	D2	D1	D0	.....	D3	D2	D1	D0
⋮					⋮				
COM239	D3	D2	D1	D0	.....	D3	D2	D1	D0
COM240	D3	D2	D1	D0	.....	D3	D2	D1	D0

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