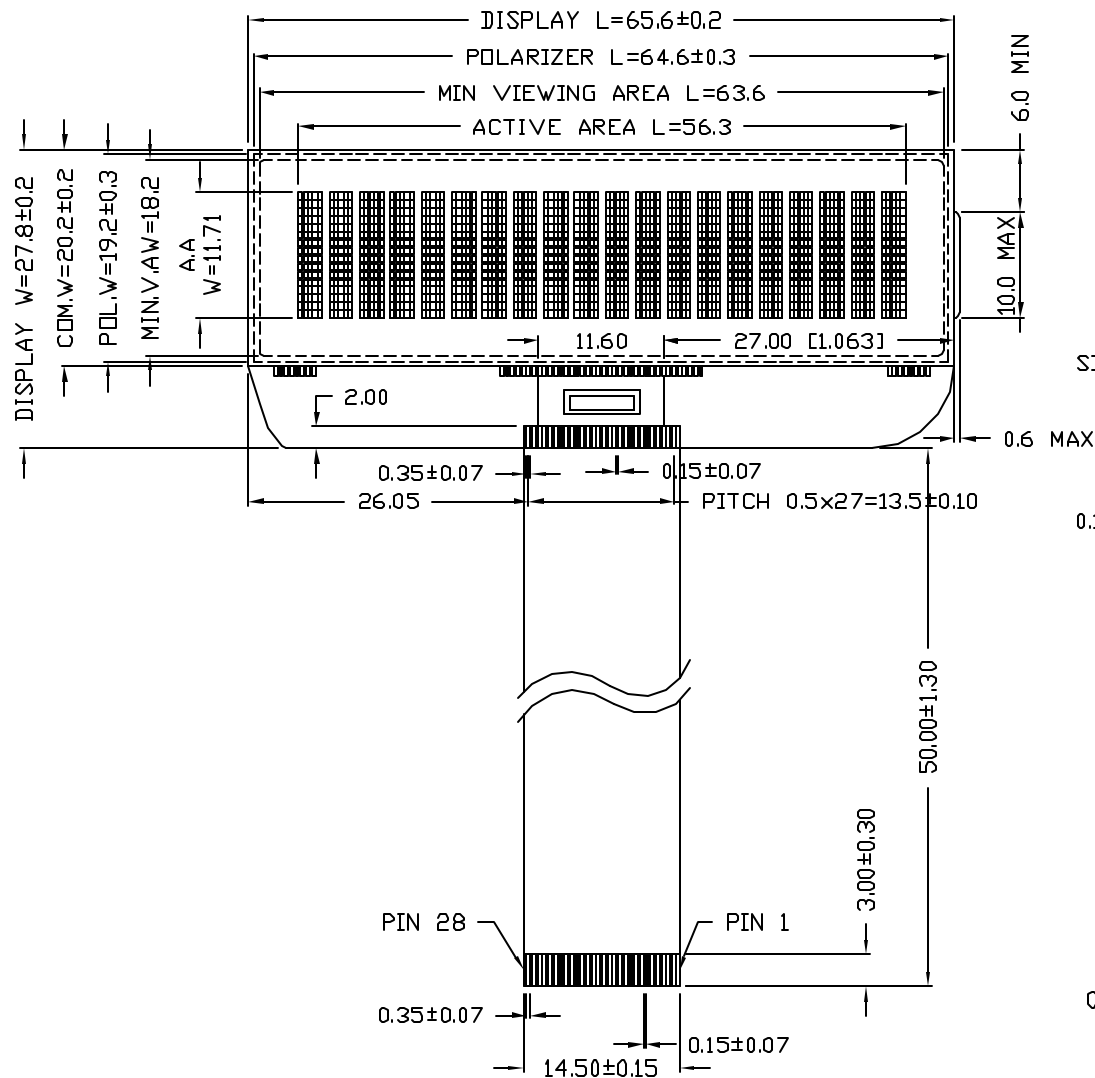


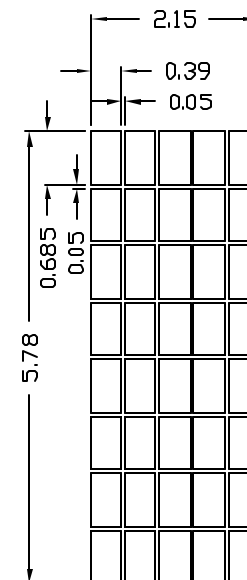
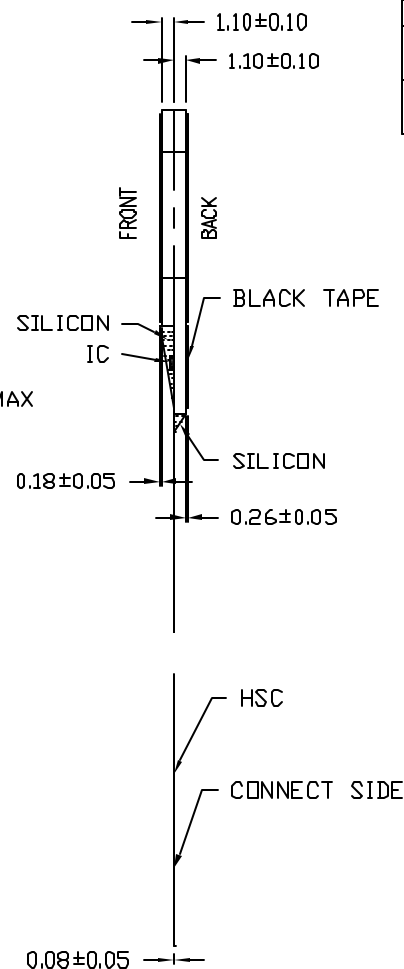
FRONT VIEW



P/N PREFIX/SUFFIX TABLE			
LCM-X	GXX	DESCRIPTION	
STANDARD	S	SR	STN, REFLECTIVE
		SF	STN, TRANSFLECTIVE
HIGH TEMP.	H	TR	TN, REFLECTIVE
		TF	TN, TRANSFLECTIVE

CAUTION: STATIC SENSITIVE DEVICE
FOLLOW PROPER E.S.D. HANDLING PROCEDURES
WHEN WORKING WITH THIS PART.

CHARACTER DETAIL



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5.78 CHARACTER HEIGHT 5 x 8 DOT MATRIX

20 X 2 C.O.G. MODULE 1/16 DUTY 1/5 BIAS 6:00 VIEW

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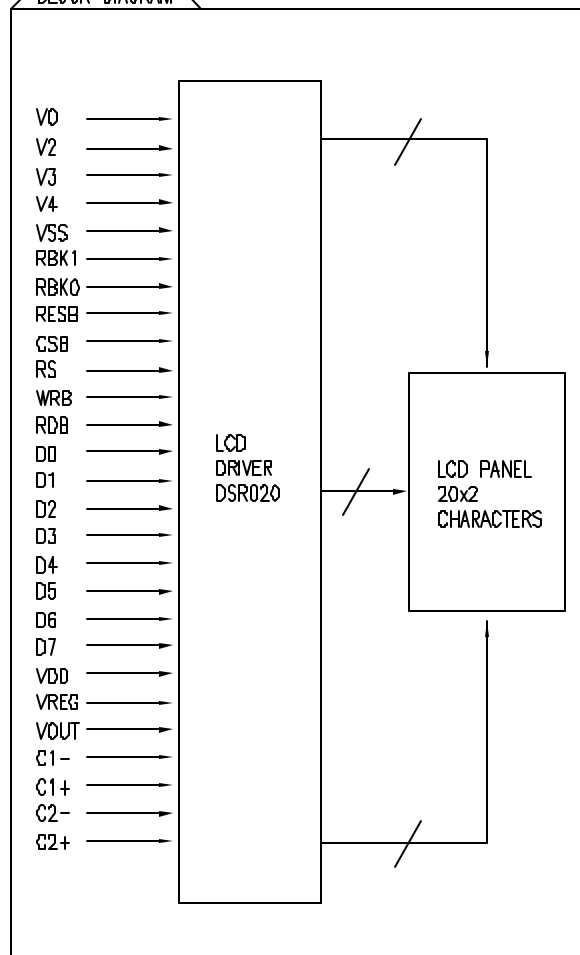
APPROVED BY:

DATE: 02.16.07

PAGE: 1 OF 1

SCALE: N/A

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

 $V_{SS}=0V$, $V_{DD}=2.7V \sim 3.3V$, $T_a=0 \sim 50^\circ C$

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN.	TYP.	MAX.	
HIGH LEVEL INPUT VOLTAGE	V_{IH}		$0.8V_{DD}$		V_{DD}	V
LOW LEVEL INPUT VOLTAGE	V_{IL}		0		$0.2V_{DD}$	V
HIGH LEVEL OUTPUT VOLTAGE	V_{OH}	$I_{OH} = -0.4mA$	$V_{DD}-0.4$			V
LOW LEVEL OUTPUT VOLTAGE	V_{OL}	$I_{OH} = -0.4mA$			0.4	V
LOW LEVEL INPUT CURRENT	I_{IL1}	$V_I = 0V$	-10		10	μA
	I_{IL2}	$V_I = 0V$	-400			μA
HIGH LEVEL INPUT CURRENT	I_{IH}	$V_I = V_{DD}$	-10		10	μA
OUTPUT LEAK CURRENT	I_{LO}	$V_I = 0V$ OR V_{DD}	-10		10	μA
LCD DRIVER OUTPUT ON RESISTANCE	R_{ON}	$ \Delta V_{on} = 0.5V$, $V_o = 6V$			TBD	$K\Omega$
STAND CURRENT	I_{STB}	$CSB = V_{DD}$, $T_{OPR} = 25^\circ C$, $V_{DD} = 3V$			TBD	μA
OSCILLATION FREQUENCY	f_{osc}	$V_{DD} = 3V$, $T_{OPR} = 25^\circ C$		230		KHz
VOLTAGE CONVERTER OUTPUT VOLTAGE	V_{OUT1}	3 x boosting, $V_{DD} = V_{EE}$, $EVOL = FH$, $R_L = 500K\Omega$ (between $V_{OUT} - V_{SS}$, internal voltage conversion)	$3V_{EE} \times 0.95$			V
	V_{OUT2}	2 x boosting, $V_{DD} = V_{EE}$, $EVOL = FH$, $R_L = 500K\Omega$ (between $V_{OUT} - V_{SS}$, internal voltage conversion)	$2V_{EE} \times 0.95$			V
CURRENT CONSUMPTION	I_{DD}	$V_{DD} = 3V$, 3 x boosting (display on)			TBD	μA

Applicable pin

- * 1 RBK1, RBK0, TEST1, TEST0, RESB, CSB, RS, P/S, M86, WRB, RDB, D0~D7 pin
- * 2 D0~D7 pin
- * 3 TEST1, TEST0, RESB, CSB, RS, P/S, M86, WRB, RDB pin
- * 4 RBK1, RBK0 pin
- * 5 APPLIES D0~D7, when internal voltage conversion
- * 6 register value when 0.5V is applied between each of SEGO~SEG99, COM0~COM15 each power supply (V0, V1, V2, V3, V4) under bias ratio 1/5.

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PIN CONFIGURATION			DESCRIPTION
PIN NO.	NAME	I/O	
1	V0	SUPPLY	Bias voltage level for LCD driving
2	V1		When using external power supply, these voltage level should be supplied after impedance change through resistor network or operational amplifier.
3	V2		In this case, voltage level should follow below condition.
4	V3		$VSS < V4 < V3 < V2 < V1 < V4$
5	V4		When choosing power circuit ON, both internal voltage booster and voltage conversion circuit generate bias voltage level on V0 to V4. In this case, a capacitor should be connected between VSS and V0~V4.
6	VSS	SUPPLY	Ground for circuit
7	RBK1	I	These pins select ROM bank to be used. They become active when "1" is written into ECR register.
8	RBK0		There are pull-up register.
9	RESB	I	Reset input. DSR020 is reset while RESB is low.
10	CSB	I	Chip select input. Low active
11	RS	I	Register selection input. When RS= "High", D0~D7 include Display RAM data. When RS= "Low", D0~D7 contain command data.
12	WRB (R/WB)	I	In 6B-series MPU interface mode This pin is connected to 6B-series MPU's R/WB pin. R/WB= "High", Read R/WB= "Low", Write
13	RDB	I	In 6B-series MPU interface mode. This pin is connected to enable Clock E signal and active high.
14~21	D0/SAL D1/SDA D2 D3 D4 D5 D6 D7/BF	I/O	When parallel interface is selected (P/S="H"), these lines become bi-directional data bus D0~D7 When serial interface is selected (P/S)="L", D0, D1 and D7 are used as SCL, SDA and BF respectively. SCL: Clock input SDA: Serial data input BF: Busy flag output At the leading edge of SCL, SDA should be shifted. At the 8th leading edge of SCL, internal circuit latches 8 bit data. After data transfer or no access, SCL must be kept low
22	VDD	SUPPLY	Power supply for logic circuit.
23	VREG	O	Output of constant voltage generation. A capacitor should be connected between this pin and VSS.
24	VOUT	O	Output of voltage booster. A capacitor should be connected between this pin and VSS.
25	C1-	O	Capacitor - connecting pin for the internal voltage booster.
26	C1+	O	Capacitor + connecting pin for the internal voltage booster.
27	C2-	O	Capacitor - connecting pin for the internal voltage booster.
28	C2+	O	Capacitor + connecting pin for the internal voltage booster.

PIN CONFIGURATION			
PAD NO	IC NO	PAD CONFIGURATION	FUNCTION
1	COM8	ROW9[C9(R1-R100)]	
2	COM9	ROW10[C10(R1-R100)]	
3	I	I	
4	I	I	
7	COM14	ROW15[C15(R1-R100)]	
8	COM15	ROW16[C16(R1-R100)]	
9	SEG99	COLUMN1[R1(C1-C16)]	
10	SEG98	COLUMN2[R2(C1-C16)]	
11	I	I	
12	I	I	
107	SEG1	COLUMN99[R99(C1-C16)]	
108	SEG0	COLUMN100[R100(C1-C16)]	
109	COM7	ROW8[C8(R1-R100)]	
110	COM6	ROW7[C7(R1-R100)]	
111	I	I	
112	I	I	
115	COM1	ROW2[C2(R1-R100)]	
116	COM0	ROW1[C1(R1-R100)]	

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MAXIMUM ABSOLUTE LIMIT				
SUPPLY VOLTAGE RANGE	SYMBOL	VALUE	UNIT	APPLICABLE PIN
	V _{DD}	-0.3 TO +4.0	V	V _{DD}
	V _{EE}	-0.3 TO +4.0	V	V _{EE}
	V _{OUT}	-0.3 TO +16.0	V	V _{OUT}
	V _O	-0.3 TO +16.0	V	V _O
	V ₁ , V ₂ , V ₃ , V ₄	-0.3 TO V _{DD} +0.3	V	V ₁ , V ₂ , V ₃ , V ₄
INPUT VOLTAGE RANGE	V _{IN}	-0.3 TO V _{DD} +0.3	V	*1
OPERATING TEMPERATURE	T _{opr}	0.3 TO +50	°C	
STORAGE TEMPERATURE	T _{stg}	-10 TO +60	°C	
OPERATING TEMPERATURE	T _{opr}	LCM-S	0~50	°C
		LCM-H	-20~70	°C
STORAGE TEMPERATURE	T _{stg}	LCM-S	-20~70	°C
		LCM-H	-30~85	°C

* 1 RBK1, RBK0, TEST1, TEST0, RESB, CSB, RS, P/S, MB6, WRB, RDB, D0~D7 PIN

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