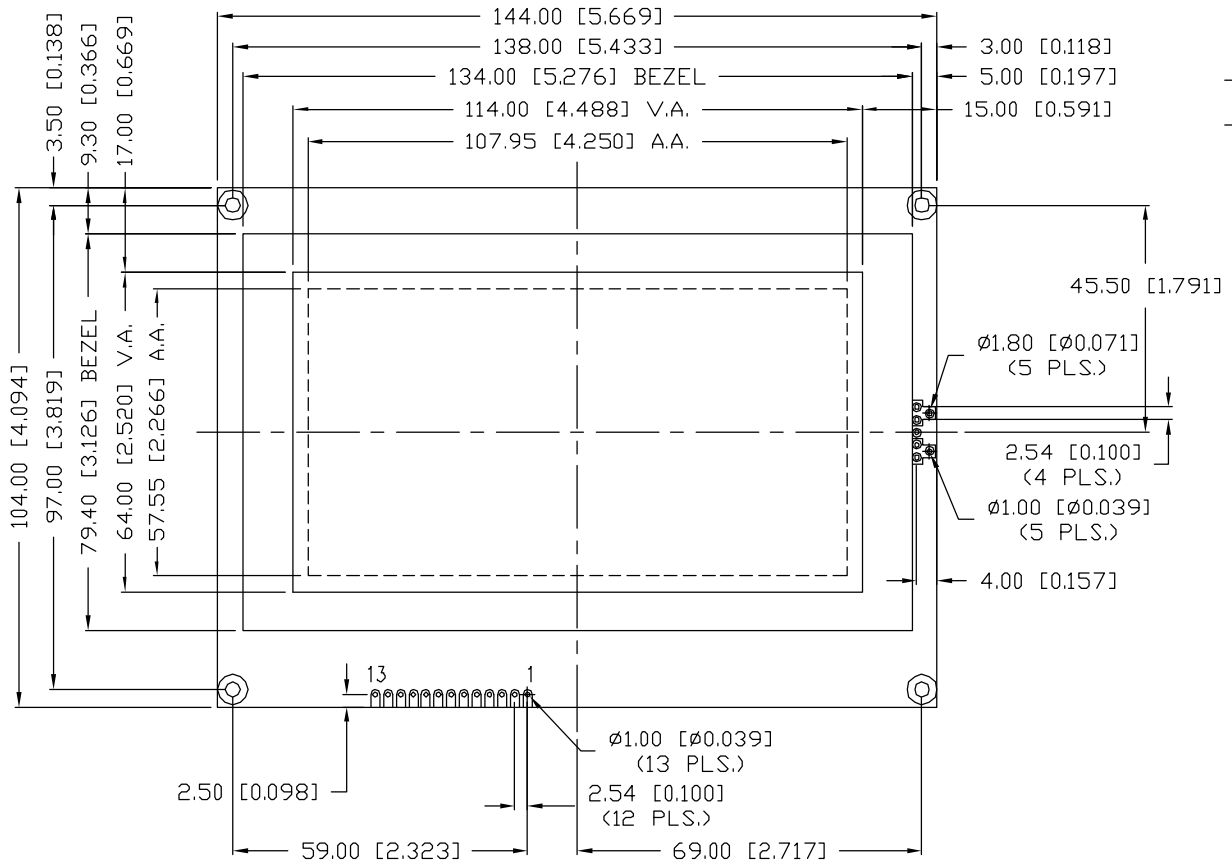
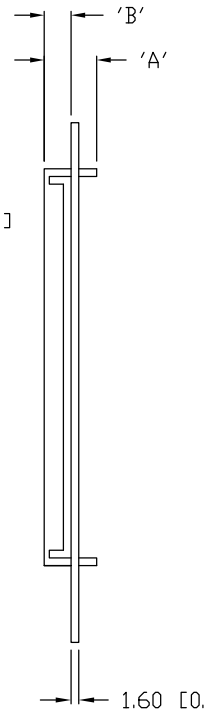
UNCONTROLLED DOCUMENT

SC:1.5	PART NUMBER	REV.
	LCM-X240128GXX/D	

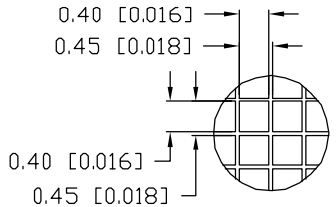
PRELIMINARY IN P/N DIR





TYPE DIM.	A	B
WITH BACKLIGHT	15.1	10.3
NO BACKLIGHT	10.0	5.2

PIXEL DETAIL



CAUTION: STATIC SENSITIVE DEVICE
FOLLOW PROPER E.S.D. HANDLING PROCEDURES
WHEN WORKING WITH THIS PART.

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REV.	PART NUMBER	CONFIDENTIAL INFORMATION	LUMEX	290 E. HELEN ROAD PALATINE, IL 60067-6976 PHONE: +1.847.359.2790 US WEB: www.lumex.com TW WEB: www.lumex.com.tw
	LCM-X240128GXX/D	THE INFORMATION CONTAINED IN THIS DOCUMENT IS THE PROPERTY OF LUMEX INC. EXCEPT AS SPECIFICALLY AUTHORIZED IN WRITING BY LUMEX INC., THE HOLDER OF THIS DOCUMENT SHALL KEEP ALL INFORMATION CONTAINED HEREIN CONFIDENTIAL AND SHALL PROTECT SAME IN WHOLE OR IN PART FROM DISCLOSURE AND DISSEMINATION TO ALL THIRD PARTIES.		
	240 x 128 GRAPHIC LCD MODULE, 5V, 1/128 DUTY, EDGE LIT LED BACKLIGHT / CCFL BACKLIGHT.	RELIABILITY NOTE OUR MANY YEARS OF EXPERIENCE DATA ACCUMULATION INDICATE THAT SOLDER HEAT IS A MAJOR CAUSE OF EARLY AND FUTURE FAILURE. PLEASE PAY ATTENTION TO YOUR SOLDERING PROCESS.	DRAWN BY: CT	CHECKED BY:

APPROVED BY:	DATE: 1.19.04 PAGE: 1 OF 3 SCALE: N/A

OPTO-ELECTRICAL CHARACTERISTICS

ITEM		SYMBOL	STANDARD VALUE			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY VOLTAGE FOR LOGIC		$V_{DD}-Vss$	4.5	5.0	5.5	V
POWER SUPPLY VOLTAGE FOR LCD: NOTE (3)		$V_{DD}-Vo$	16.9	18.0	19.2	V
INPUT VOLTAGE: NOTE (1)	H LEVEL	V_{IH}	2.2	–	–	V
	L LEVEL	V_{IL}	0	–	0.6	V
OUTPUT VOLTAGE: NOTE (2)	H LEVEL	V_{OH}	2.4	–	–	V
	L LEVEL	V_{OL}	0	–	0.4	V
POWER SUPPLY CURRENT FOR LOGIC: NOTE (4)		I_{DD}	–	15	24	mA
POWER SUPPLY CURRENT FOR LCD DRIVE: NOTE (4)		I_{EE}	–	5.0	–	mA
CLOCK OSCILLATION FREQUENCY		fosc	–	5	–	MHZ

*ONLY APPLIES TO MODULES WITH BACKLIGHT

NOTE (1): APPLIED TO TERMINALS: FS, CE, $\overline{WR}$, $\overline{RD}$, C/$\overline{D}$, DB0~DB7, $\overline{RES}$, MD2.

NOTE (2): APPLIED TO TERMINALS: DB0~DB7.

NOTE (3): RECOMMENDED LCD DRIVING VOLTAGE MAY FLUCTUATE ABOUT ±1.0V BY EACH MODULE.

NOTE (4): $V_{DD}-Vss=5.0V$, $V_{DD}-V0=20.6V$.

ABSOLUTE MAXIMUM RATINGS

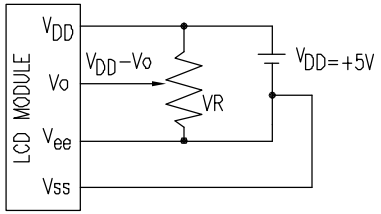
ITEM	SYMBOL	TEST CONDITION	STANDARD VALUE		UNIT
			MIN	MAX	
SUPPLY VOLTAGE FOR LOGIC	$V_{DD}-Vss$	–	0	7.0	V
SUPPLY VOLTAGE FOR LCD DRIVE	$V_{DD}-Vo$	–	0	28	V
INPUT VOLTAGE	V_I	–	Vss	V_{DD}	V

PIN CONFIGURATION

PIN #	SYMBOL	LEVEL	FUNCTION
1	FLM	–	FIRST LINE MARKER
2	M	H/L	CONTROL SIGNAL FOR AC DRIVING
3	LP	H->L	COMMON DRIVER DATA SHIFT SIGNAL
4	CP	H->L	CLOCK PULSE FOR SEGMENT SHIFT REGISTER
5	VDD	–	POWER SUPPLY FOLTAGE
6	Vss	–	POWER SUPPLY GROUND
7	VEE	–	POWER SUPPLY VOLTAGE FOR LCD
8	DB0	H/L	DATA BIT 0
9	DB1	H/L	DATA BIT 1
10	DB2	H/L	DATA BIT 2
11	DB3	H/L	DATA BIT 3
12	Vo	–	CONTRAST ADJUSTMENT VOLTAGE
13	NC	–	NO CONNECTION

$V_{DD}-Vo$: LCD DRIVING VOLTAGE

VR: 10KΩ-20KΩ



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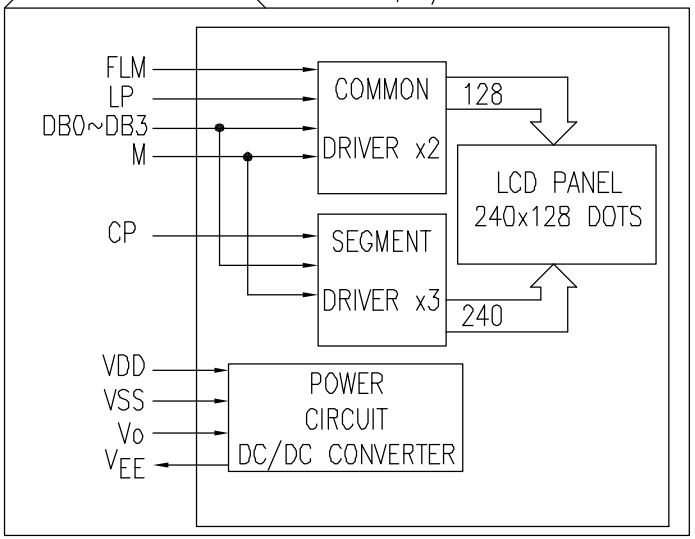
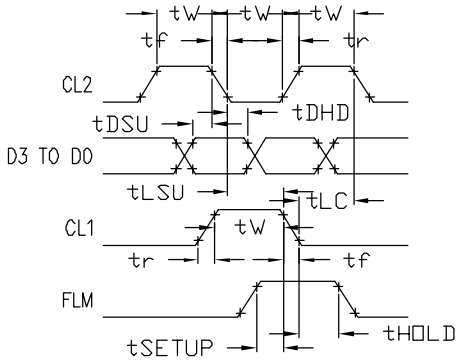
PRELIMINARY IN P/N DIR

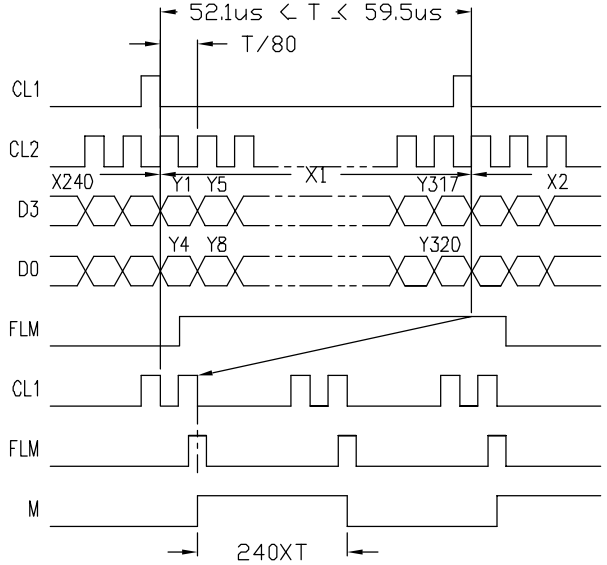
BLOCK DIAGRAM 240 x 128, 1/128 DUTY





TIMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
CLOCK FREQUENCY	f_{CP}	–	8	MHz
CLOCK PULSE WIDTH	t_W	45	–	ns
RISE, FALL TIME	t_R, t_F	–	15	ns
DATA SET-UP TIME	t_{DSU}	20	–	ns
DATA HOLD TIME	t_{DHD}	20	–	ns
CL1 SET-UP TIME	t_{LSU}	80	–	ns
CL1 -> CL2 TIME	t_{LC}	80	–	ns
FLM SET-UP TIME	t_{setup}	100	–	ns
FLM HOLD TIME	t_{hold}	100	–	ns
M DELAY TIME	t_{DF}	–	300	ns



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CT			PAGE: 3 OF 3
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